Multilevel Boost Converters, their Applications, Comparison and Practical Design Aspects

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Abstract— **The need for renewable and more efficient electrical energy generation, distribution and conversion drives exploration of new power conversion topologies and development of advanced power component technologies. Recently reintroduced multilevel boost converter topologies, by allowing use of new, efficient but relatively low voltage power devices at higher voltage and power levels, are becoming popular solution in industrial and transportation power systems. The paper compares key design parameters of multilevel boost converters with separate loads, fly capacitor and clamping diodes. It provides recommendations for emerging component base for such applications. Practical design recommendations for efficient and high power density three-level boost converter supported by test results are provided based on suggested analysis.**

Keywords-component; multilevel converter; boost conveter; DC-DC converter

I. INTRODUCTION

Traditional, well known, non-isolated boost converter [1] is widely used in single-, three-phase and interleaved PFCs and switching regulators to supply higher voltage loads from available lower voltage power sources. Recently, their applications expanded into renewable, "green power" generation and distribution systems, transportation and vehicular powertrain systems to generate high voltage DC bus. Broadening power conversion tasks and more demanding requirements have forced a search for other boost topologies that allow miniaturization, increased efficiency and reduced system cost. Such search is also supported by emerging wide bandgap SiC and GaN power devices, as well as the technology advances in the area of control, driver ICs and passives.

Non-isolated boost topologies, other than traditional boost converter (BC), have been considered in the literature, including various multilevel converters. Three-level BC topologies were considered for three-phase rectifier in [2] and for single-phase PFC in [3]. Four-level one- and two quadrant DC-DC converters were proposed in [4]. Two quadrant converters might be used as one directional device with many

useful boost features of that circuit but authors did not indicate such possibility. Paper [5] presents an analysis and evaluation of a two-switch boost rectifier operating in a three-phase system in discontinuous conduction mode (DCM). The harmonic distortion in two-switch topology is lower than created by single switch three-phase DCM boost rectifier. A new topology of interleaved three-level boost converter (TLBC) with coupled inductors to reduce input current ripple and possibly EMI is proposed in [6]. In [7] three-level version of flying capacitor boost converter (FCBC) topology is used in low power PFC. Flying capacitor multilevel boost topology was initially developed for high power applications in industrial products in few kV and MW power range. Nowadays, the multilevel topologies are used in various applications. In [8] authors present an analysis of the Active Neutral-Point-Clamped five-level converter (ANPC5L) with regards to total harmonic distortion reduction in high speed, high power applications. ZVT PWM three-level BC for PFC is proposed in [9]. In fact the presented circuit operates as two interleaved conventional boost converters. Only one auxiliary switch is needed for active soft switching circuit. Three-phase PV system with TLBC using maximum power point tracking (MPPT) control is presented in [10]. The TLBC reduces reverse recovery loss in diodes that is demonstrated by experimental results based on 10 kW prototype operating at 10 kHz. In this TLBC power switches operate without overlapping. Paper [11] discusses in details two solutions of isolated DC-DC converters for auxiliary railway power supply. Nominal input voltage is 3000 VDC. One of the considered topologies contains the TLBC module followed by half bridge zero-current switching (HBZCS) PWM converter. Capacitors of the TLBC are part of resonant process of the HBZCS, so they should be quite small. Experimental validation of the analysis has not been carried out. Nevertheless, authors make a conclusion that the auxiliary converter with the TLBC and HBZCS cannot operate correctly in the whole range of the DC input voltage (2,2 … 4,0 kV). This statement is challenged by more detailed analysis and practice. Three-level converters based on diode clamped three-level inverter were described in [12]. A wide family of three-level converters has been derived.

However, shown in the paper TLBC (Fig. 4(b)) has to be actually classified as two-level topology where the diode clamp does not work properly in one of the main operating modes. Two-stage TLBC operating in PV energy generation station shown in [13]. The output of TLBC supplies two PWM inverters operating with phase shift. Paper [14] describes multilevel BC operating with renewable energy sources. The paper deals with DC-DC boost converters called by the authors as vertical interleaved topologies. Authors consider in details four- and five-level converters with different control strategies of power switches including options with ZVS. A conclusion is made based on modeling of four-level boost converter with parameters: Vin = 800 V, Vo = 3 kV, Po = 150 kV. In [15] distributed PV plant architectures are considered as replacement for the classical central inverter based system. In such systems converters with very high efficiency and simple topologies are required for cost effective solution. The use of TLBC topology is suggested to meet the requirements instead of conventional BC. The paper [16] highlights two stage architecture of a utility scale PV power system. Two 500 kW three level DC-DC boost converters are developed as a part of one MW utility scale system. Output power of the converters is maximized and the grid disturbances are controlled effectively by grid connected inverter. Each converter operates from separate PV panel with an input voltage 1050 V. Two level output inverter supplies 690 V AC mains. Paper [17] presents analysis of TLBC operation in two modes and shows several advantages versus traditional BC. It is demonstrated that the size and power losses in the choke of the TLBC are lower than those of traditional BC. Small-signal models of TLBC for both modes in continuous conduction mode are provided. Critical design considerations for regulated systems with feedback loop including start-up process are provided in details. This brief review of multilevel BC related publications above demonstrates growing interest to these topologies because of expected better performance versus traditional BC in high voltage and high power applications.

This paper is organized as follows. More detailed application examples of boost converters as part of power system and related requirements are discussed in Section II. Section III focuses on new technology developments in the area of active power devices, passives, controller and driver ICs that simplify implementation of new multilevel boost converter topologies and allow achieve maximum performance. Section IV introduces modification of traditional BC to address higher voltage and power needs. Section V analyzes key parameters of flying capacitor three-level BC. The authors were not able to find recommendations how to get maximum gain of transfer ratio for any multi-level topologies in the literature. Also, the detailed analytical comparison of flying capacitor and clamped diode multi-level boost converters is needed for design purposes. The analysis provided in Section VI tries to address these important issues. Section VII expands the analysis into higher level, four and more, topologies. This paper also shows experimental data of two TLBC converters, one designed for relatively low input voltages (some tens volts), and the second intended to be used with input voltages as high as several kV.

II. POWER SYSTEMS WITH BOOSTED DC VOLTAGE

Driven by environmental protection agencies and climate saving initiatives worldwide, the renewable sources for electrical energy generation are gaining popularity [18]. The major sources of renewable energy, like solar panels, wind turbines and fuel cells, produce maximum power only at specific optimal operating point that usually does not allow direct connection to grid [19]. Thus, these energy sources, backed up by energy storage elements, like, for example battery, are connected to the electrical grid through additional power conversion stages. For the commercial and residential buildings with voltages less than 1000V and power less than 1 MW, hybrid system with intermediate DC Bus is popular solution (Fig.1). This DC Bus through single inverter is connected to the electrical grid. Such electrical system requires few boost DC-DC converters because optimal voltages at the outputs of energy sources and storage batteries are usually much lower than needed for the connection to grid [16].
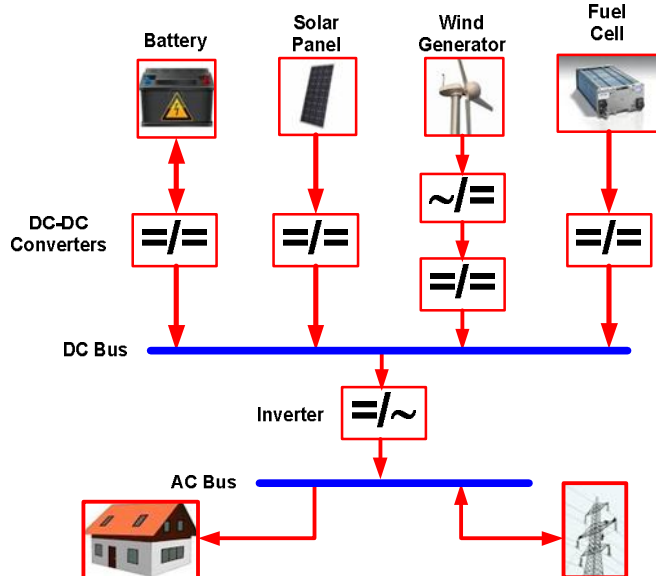

Figure 1. Electrical power generation and distribution system with intermediate DC Bus

Another popular application for high gain boost DC-DC converter can be found in transportation electrical systems, where boost converters generate high voltage for traction motor drives from lower voltage battery sets [20]. Simplified block diagram of hybrid electrical vehicle (HEV) powertrain is shown in Fig.2. The DC-DC converters between automotive batteries and motor/generator inverters must be bidirectional to supply motor in forward drive mode and to charge the batteries during operation in reverse break mode. Converters for HEV and electrical vehicles (EV) must be efficient and high power density to minimize overall weight and increase driving distance without re-charging and re-fueling. Also, strict environmental operating conditions must be met to qualify for automotive applications. One example of such commercial product is BDC546 bidirectional DC-DC converter from Brusa. This converter achieves 98.9% efficiency and 6.4 kW/kg power density at 400 V input voltage, 600 V output voltage and 120 kW continuous output power. Converter is using liquid cooling

for temperature management and operates at 39 kHz switching frequency [21]. There are applications where even higher, at least few kV output, boost converters are required [14] [17].
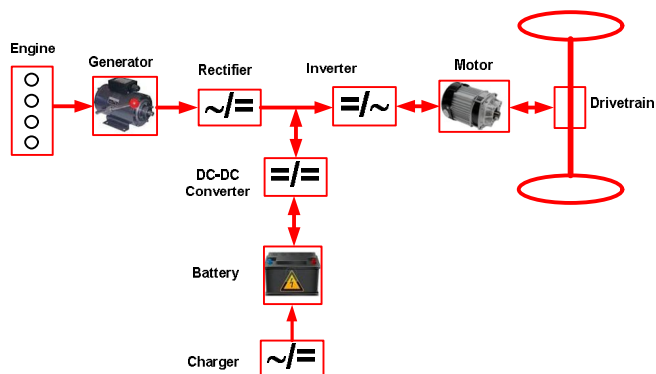

Figure 2.   Power conversion and flow in HEV powertrain

It is critical to minimize cost and size of high voltage and power boost converters while increasing the efficiency. Traditional high voltage power devices, like IGBT or GTO, used in such applications, operate at relatively low frequency, usually 5 to 20 kHz. Low frequency operation requires large and bulky magnetics and capacitors for filtering and conversion and it also generates audible noise. Some applications, like converters for vehicle powertrain, benefit from ability to operate at high temperatures 200°C and above, and at high frequency to increase power density. Based on these considerations, since 70-s, multilevel converter topologies were proposed allowing use of lower voltage and cost, faster switching devices for high power and voltage applications. Multilevel topologies have become even more attractive lately, after wide band gap GaN and SiC power devices have become commercially available, but their voltage and power range is still limited. Appearance of high quality film capacitors and new magnetic components also support the drive for better efficiency, lower cost and size boost converters. Because of increased number of power devices involved in multi-level topologies, availability of adequate controller ICs and isolated driver solutions becomes critical as well. The recent technology advances on component level are reviewed in the next section.

III.   NEW POWER COMPONENTS SUPPORT TOPOLOGY INNOVATIONS

A.   Wide Bandgap Power Devices

Wide bandgap semiconductor materials like GaN, GaAs, SiC exhibit combination of parameters, shown in Table 1, that potentially make them better fit for power devices versus Si. Semiconductor material parameters like breakdown voltage Vbr, mobility μe, bandgap Eg, relative dielectric constant ε_r determine theoretical limits of specific on resistance per die area at specified voltage rating of the device, as it is shown in Equations (1) and (2) derived in [32]. Equation (1) addresses indirect bandgap materials like Si and SiC. Equation (2) is for direct bandgap materials like GaN. Specific resistance using these equations are in mΩ•mm^2.

TABLE I.   KEY PARAMETERS OF POPULAR SEMICONDUCTOR MATERIALS

Material	Si	GaAs	InP	GaN	4H-SiC
Bandgap, eV	1.1	1.43	1.35	3.4	3.26
Breakdown Field, V/μm	30	40	50	300	200-<300
Electron Mobility, cm^2/Vs	1500	8500	5400	1500	700
Saturated Electron velocity, 10^7 cm/s	1	<1.0	1	1.3	2
Peak Electron velocity, 10^7 cm/s	1	2.1	2.3	2.5	2
Thermal Conductivity, W/cmK	1.3	0.55	0.68	>1.5	<3.8
Lattice Constant (a), A	5.43	5.65	5.87	3.19	3.07
Dielectric Constant, ε_r	11.7	12.9	12.5	9	9.7

$$Ronspi = \frac{3.351 \times 10^2 \times Vbr^2 \times Eg^{-6}}{\mu e \times \varepsilon_r} \qquad (1)$$

$$Ronspd = \frac{8.725 \times 10^2 \times Vbr^2 \times Eg^{-7.5}}{\mu e \times \varepsilon_r} \qquad (2)$$

Based on this, theoretical limit plots have been determined for different semiconductor materials and technologies that are shown in Fig. 3.
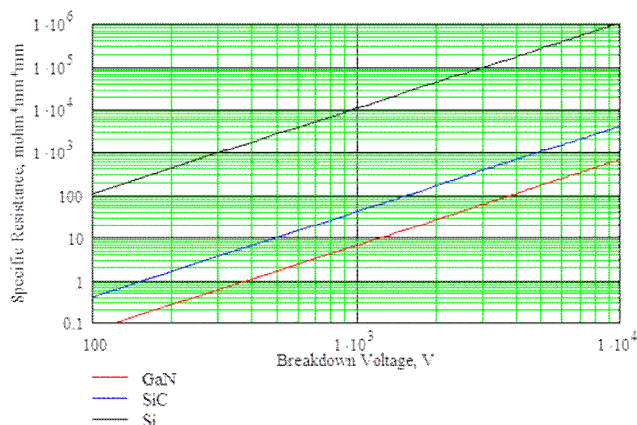

Figure 3.   Specific Ron resistance versus breakdown voltage

From these plots, for power device rated at 1000 V, the specific resistance of Si FET is 250 and 1400 times respectively higher versus SiC and GaN FETs. Certainly, performance of currently available SiC and GaN power devices is far from theoretical limit and significant efforts are under way to improve the process, manufacturability and yield at lower cost. But even early commercial samples show impressive performance. The SiC power devices also demonstrate better performance at high temperatures versus Si that make them perfect choice for applications like drilling, airspace, electrical energy production and conversion, transportation (Table 2). Production of SiC and GaN power devices is growing about 38% per year [22] and higher volumes will gradually drive the cost down. However, introduction of new technology does not mean simple replacement of Si based devices by SiC or GaN. Successful implementation is only possible with availability of specialized

driver and controller circuits, magnetic materials and capacitors

capable to operate at higher frequency.

TABLE II.   KEY PARAMETERS OF COMMECIALLY AVAILABLE SiC POWER FETS

Vendor	Part	Vds, V	Id, A	Vg, V	Rdson, mΩ	Qg, nc	FM, mΩ•nc	Die size, mm x mm	Spec. Ron. mΩ•mm^2
Cree	CPM2-1200-0080B	1200	20	+25/-10	80	49	3920	3.36x 3.1	833
Cree	CPM2-1200-0025B	1200	50	25/-10	25	179	4475	6.44x4.04	650
Rohm	SCT2080KE	1200	35	+22/-6	80	106	8480	TO-247	n/a
GeneSic	GA50JT12-247 (bipolar)	1200	50	3.3V, 2A	28	n/a	n/a	TO-247	n/a
MicroSemi	APTMC120AM55CT1AG	1200	55	+25/-10	49	98	4802	Module	n/a
ST Micro	SCT30N120	1200	45	+25/-10	80	105	8400	HiP247	n/a

The optimization on system level including new topologies analysis and development is equally important.

B. Wide Bandgap Power Devices Oriented Driver Solutions

Wide bandgap power devices technology is in its introductory stage and this means large diversity of approaches taken by manufactures. FET devices include not only normally OFF, but also normally ON variations, i.e. JFETs. There are also SiC BJT power devices in the market. Even normally OFF devices require wide variety of drive voltages like, for example, 5 V for GaN FETs from EPC [23] to 20 V for SiC FETs from Cree [24]. Driver IC vendors follow the trend and introduced driver circuits optimized for specific power device. For example drivers LM5113, LM5114 and UCC27611 from Texas Instruments are optimized for GaN FETs from EPC, while UCC27532 driver from the same company is optimized for use with SiC FETs. Multilevel topologies also require controllers with multiple PWM outputs. Digital controller families C2000 and UCD3K from Texas instruments simplify implementation of optimal control strategy [25]. To illustrate the driver circuit solutions, we consider the following example.

In most cases, power conversion topologies include power devices in half-bridge, full-bridge, multi-phase or other various configurations connected in series and requiring separate isolated bias supply for each driver and related switch. As an example, the simplified block diagram of three-level inverter topology, is shown in Fig. 4.
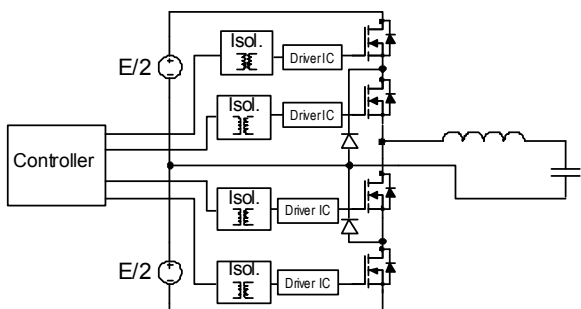

Figure 4.   Three-level inverter with signal and bias isolation for driver ICs

In this diagram every FET has its own driver IC. Interface between the controller and driver is provided by isolated bias supply using transformers for power and signal isolation. In practical design, power device might need different voltages to turn on and turn off. In this case, split output rail bias supply is

used or two separate bias supplies are needed per each power device. Example of such solution is shown in Fig. 5.
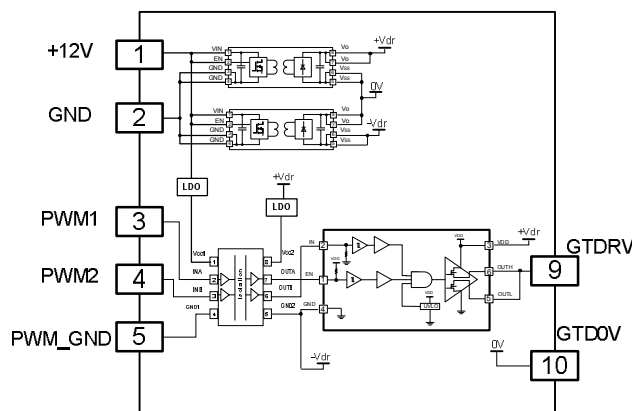

Figure 5.   Electrical diagram of complete isolated driver solution

The circuit includes two isolated bias supplies with transformers, one for turning on power switch, and the second for turning off, signal isolator that could use either opto-coupler, capacitive or transformer based isolation, and driver IC. For fast switching wide bandgap devices, the signal isolation based on integrated capacitors or transformers is preferable versus opto-couplers because of shorter propagation delays with much less variations over process and temperature. There are various implementations of isolated driver circuit currently used in industry depending on power and isolation requirements and integration levels. One example of such board is shown in Fig. 6.
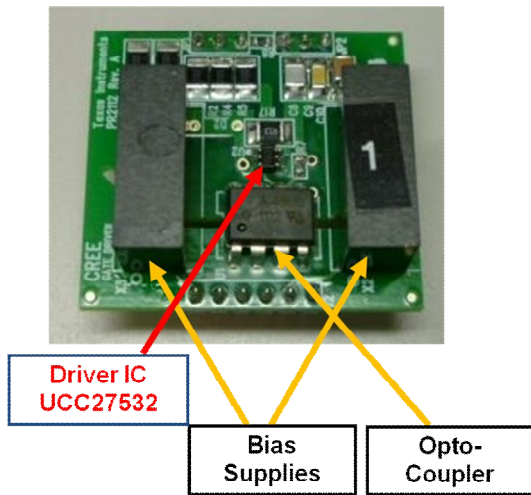
Figure 6.   Isolated driver board

The size of this board is 38 mm x 36 mm x 12.5 mm. Most of the area and volume are occupied by bias supplies and signal isolator. In this case, the bias supplies are based on discrete components and transformers assembled on special lead frame and molded by compound to form isolated bias supply in package. The trend in industry is towards size and cost reduction of isolated bias supplies by using higher level of integration and advanced IC manufacturing processes. Thus, the development of integrated on wafer bias supplies with transformers becomes important direction in technology development [26]. There is also trend to integrate driver IC and signal isolator to compile isolated driver. This approach is gaining popularity because it makes driving power devices independent on selected topology [27].

C.   Development of High-frequency High-voltage Capacitors

Many applications in high power, high voltage system require 15 or even 20 years of lifetime. This is especially important for renewable energy based power distribution and conversion. Thus, the use of popular electrolytic capacitors in such applications is undesirable because of relatively short life time. The trend is by using higher frequency operation implementing multilevel topologies as long as new and better performance power devices significantly reduce the size of passives, including capacitors. This allows the use of film and ceramic capacitors instead of bulky and less reliable electrolytic capacitors. Comparison of dielectric materials for capacitors and efforts to increase their energy density is provided in [28].

D.   Development of New High-frequency Magnetic Materials for High-power Applications

Minimizing losses in magnetics and reducing their size is critical for efficient, high power density and low cost power conversion. The size of magnetics can be reduced by increasing the operating frequency. This is proven widely for low power applications where the frequency sometimes is risen up to MHz frequency range. For high power and voltage power conversion the operating frequency is limited to few kHz, primarily because of switching losses in power switches and magnetic core and windings. The use of new topologies and power

devices allows increase operating frequency and significantly reduce the size of magnetics provided that new magnetic materials are capable to operate at large flux density with minimum power losses. Recently, new nano-crystalline magnetic materials are come under consideration for such applications, although their cost is relatively high versus traditional materials like ferrite and even amorphous [28].

IV.   MODIFIED BOOST TOPLOGY

Modifications of conventional non-isolated BC are possible still retaining and even improving its important features. Modified boost topology (MBT) with separated loads R1 and R2 is shown in Fig.7. Such topology, called power cell, by itself has limited practical value. But it allows connect in series multiple cells to supply numerous separated loads. The diodes D2 and D3 provide separation between loads. The MTB remains a step-up topology because main operation features of BC are preserved. The topology uses a vertical multilevel principle. Switches S1 and S2 can operate with and without overlapping.
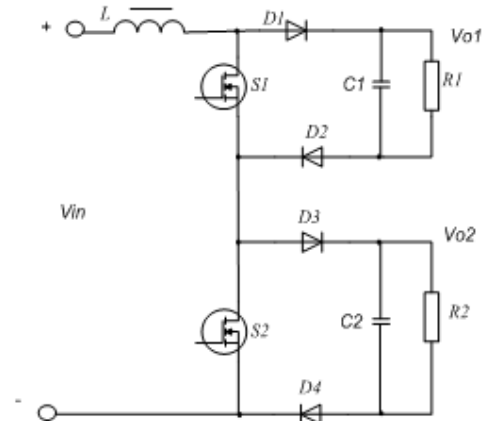

Figure 7.   Modified boost topology with two loads

Because the circuit has a vertical symmetry, the whole switching cycle can be divided into two equal half-cycles between switches S1 and S2, where each of them has an interval of accumulating energy in the choke followed by interval of freewheeling. If there is no overlapping condition, both switches during freewheeling are open, and the choke delivers energy to the capacitors and loads. If overlapping is allowed, then four different conditions are possible: both switches are on, both switches are off and two conditions when one of the switches is on and the other off. Described circuit can be expanded to include N stages that can also operate with and without overlapping. Steady state transfer function ratio (TFR) of circuit depends on number of stages, duty cycle and modes of operation. This N-stage topology allows the use of low voltage rated power devices with much higher input voltage for the converter.

V.   THREE-LEVEL FLYING CAPACITOR BOOST CONVERTER

There is other version of multi-level BC called flying capacitor boost converter (FCBC). The earliest found reference to this technique is dated 1992 [31]. Three-level variant of this

topology (TLFCBC) is shown in Fig. 8. Steady state and small signal modeling of the circuit is provided in [29] and [30]. In this paper some additional considerations related to modes of operation are added.
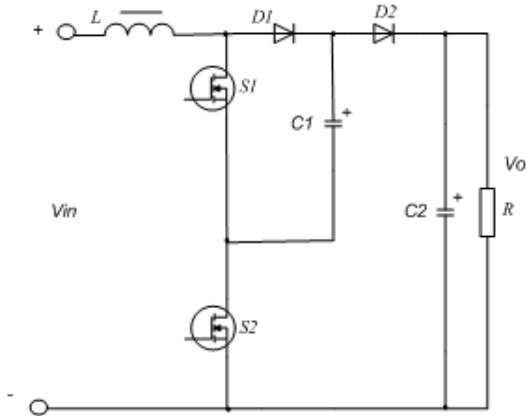

Figure 8. Three-level flying capacitor boost converter

Power switches in FCBC can operate with and without overlapping .

When operating without overlapping, let us assume the switch S2 is closed and switch S1 is open at first half switching cycle. At this condition the voltage difference between input Vin and voltage at capacitor C1 is applied to the choke and it accumulates energy while capacitor C1 is charged. During the second half of switching cycle, the switch S2 is open and switch S1 is closed. The voltage at the choke equals to the voltage at capacitor C2 minus voltages at capacitor C1 and Vin. During the second half switching cycle again the switch S2 is closed and the switch S1 is open for the same duration of time as during first half cycle. At the stage of delivery energy from the choke both S1 and S2 are open. The voltage applied to the choke is equal to the difference between the voltages Vo and Vin. The symmetry of the circuit in both halves of the switching cycle requires that the voltage at the capacitor C2 is twice as much of the voltage at the capacitor C1. Thus, steady state transfer ration (TFR) of the circuit in this operation without overlapping is:

$$V_o = \frac{2V_{in}}{2-D}. \tag{3}$$

Where: $D = 2t_i / T$ - a duty cycle changing from 0 to 1; T – the switching cycle of operating one of the switches. When the TLFCBC operates with the overlapping of the switches, there are two switching strategies shown in Fig. 9. The first strategy has at least one switch conducting during pause p1 (Fig. 9a). In the second strategy there is additional pause p2 when both switches are open (Fig. 9b).
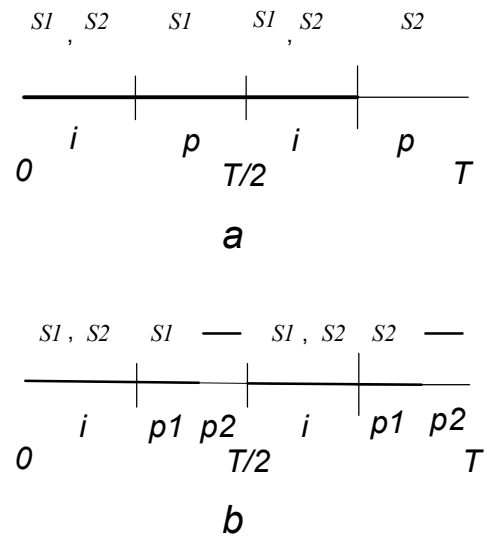

Figure 9. Two overlapping switcing strategies: a) at least one switch conducts during pause p1, b) additional pause p2 when both switches are open

In Fig. 9, T is the switching cycle. For the first strategy TFR for continuous choke current is:

$$V_o = \frac{2V_{in}}{1-D}. \tag{4}$$

The second strategy (Fig. 9b) yields the following TFR:

$$V_o = \frac{2V_{in}}{(1-D)(2-k)}. \tag{5}$$

Where k – quotient showing which part of a full pause ($P = P1 + P2$) occupies the interval $P1$, that is $D1 = k(1-D)$. The quotient $k \in 0...1$; for $k = 0$ $P = 1-D$ and the circuit in Fig. 8 operates as the conventional BC. When $k = 1$ the strategy two (Fig. 9b) changes to strategy one (Fig. 9a). Under any the value k between o and 1 TFR of the circuit Fig. 8 allows to get worse gain than in case when the circuit works accordingly to strategy 1. Also, the switching frequency of each switch under the strategy 2 is twice as much in comparison with the strategy 1. So, the strategy 1 is preferable.

Now, let us consider operation of the capacitors. First of all, they have different values of working voltages: C1 operates at Vo/2 and C2 at Vo. Secondly these capacitors work with different currents because the capacitor C1 conducts the currents of choke during pulse and pause. The operation of the choke, switches and diodes occurs in more favorable conditions than in the BC: the ripple of the current of the choke is much less and voltages at the switches are half of the conventional BC.

VI.   THREE-LEVEL BOOST CONVERTER

A.   Operating modes and related transfer ratios

The electrical diagram of three-level boost converter (TLBC) is shown in Fig. 10.
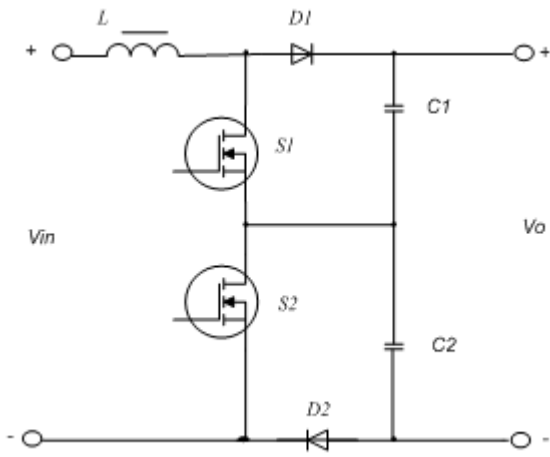
Figure 10. Three-level boost converter

This topology pursues the same goal as the TLFCBC described in the previous section – to boost the output voltage using lower voltage rated components versus standard boost converter. The topology is capable to increase the output voltage eight times or more versus the input voltage. Switches in the TLBC may work with different algorithms and the simplest one of them repeats the switching algorithm of BC. Hereinafter, we'll consider two main modes – without overlapping of the switches – mode 1 and with overlapping – mode 2. For the mode 2 (with overlapping) there are possible two sequences (sub-modes) which have been described for the TLFCBC (Fig. 9a and Fig. 9b). Because the sequence 2 (Fig. 9b) requires doubled switching events of transistor within switching cycle and TFR, similar to TLFCBC, is smaller versus for the sequence 1, further we will discuss only modes without overlapping and the sequence 1 with overlapping. The waveforms of two operating modes in consideration are shown in Fig. 11.
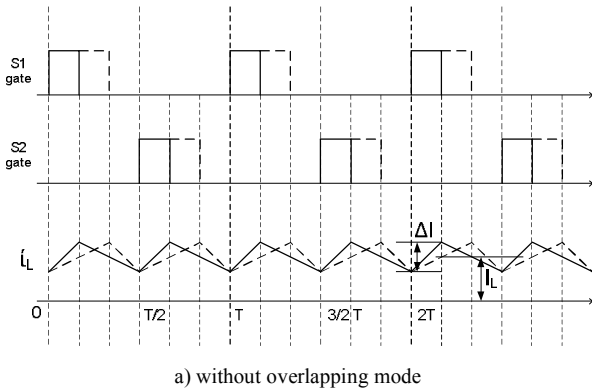
a) without overlapping mode
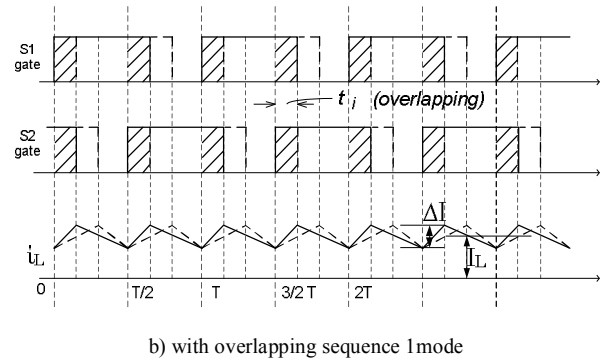
b) with overlapping sequence 1mode

Figure 11. Waveforms of two operating modes for TLBC

Compared to the standard BC the switching frequency of the TLBC can be as follows:
1. Frequency of each switch in the TLBC is higher than the frequency of switch in the BC.
2. The frequency of each switch in the TLBC equals frequency of the switch in the BC.
3. The frequency of each switch in the TLBC is lower than the frequency of the switch in the BC.
Each of these options has advantages and drawbacks. Option 1 reduces the size of the choke greatly, but the switching loss in power devices and diodes increase over frequency. Still, because of lower voltage rated devices used in TLBC, the overall efficiency can be higher than in standard boost.
Option 2 was investigated in [3], where TLBC was used in the single-phase PFC). It was shown that the choke size is smaller versus standard BC and power loss is lower versus version 1.
It is obvious that the switching loss in option 3 will be the lowest but it is unclear what will be the size and loss of the choke compared to the standard BC. The analysis in this paper focuses on option 3 with assumption that the operating frequency of each switch in the TLBC is half of the frequency of the switch in the BC. With this assumption the choke in TLBC operates at the same frequency as in the standard BC.

For both operating modes we get the following expressions for the TFR of the TLBC.

Mode 1 (without overlapping):
$$V_o = 2V_c = 2V_{in}/(2-D). \qquad (6)$$

Where: V_c - voltage across each capacitor;

$D = 2t_i/T_{SW.TLBC}$ - duty cycle for mode 1;

$T_{SW.TLBC} = 2/f_{sw}$ - the switching cycle in mode 1;

f_{sw} - the switching frequency in the BC.

Mode 2 (with overlapping):
$$V_o = 2V_c = 2V_{in}/(1-D). \qquad (7)$$

Where: D in this equation is defined as D for mode 1.
Output voltage for conventional BC is as follows:
$$V_o = V_{in}/(1-D) \qquad (8)$$

Comparison of TFR of TLBC versus conventional BC demonstrates considerable differences.

Firstly, in without overlapping mode, V_o cannot be more than twice of V_{in} even for D→1. It is a serious restriction for a number of applications, while it is very convenient for others. The example of such application will be discussed in next section.

Secondly, in the overlapping mode, V_o is twice as higher than in standard boost converter for the same duty cycle D. Therefore, higher output voltage can be achieved with higher density and efficiency.

B. Operation of the choke in TLBC

The choke is critical component both in BC and TLBC. The success of a design depends on the size, loss and cost of this component. Therefore, let us consider in detail the peculiarities of choke operation in BC and the TLBC, taking into account that for TLBC operating at half of BC switching frequency, the choke operates at the same frequency as one in BC.

Firstly, we determine the current ripple in the choke for different V_o / V_{in} ratios. For the BC:

$$\Delta I = V_o (1 - V_{in} / V_o) V_{in} / V_o / (L f_{sw}) . \quad (9)$$

For the TLBC operating without overlapping:

$$\Delta I_1 = V_o (1 - V_{in} / V_o)(2 V_{in} / V_o - 1)/(L f_{sw)}) . \quad (10)$$

For the TLBC operating with overlapping:

$$\Delta I_2 = V_o (V_{in} / V_o)(1 - 2 V_{in} / V_o)/(L f_{sw)}) . \quad (11)$$

From (9) through (11) one can see that ΔI_{max} of the BC choke is twice as high for the same value of choke in the TLBC operating either with, or without overlapping. This means it is possible to make the choke of the TLBC smaller compared with the BC although the operating frequencies of the chokes are the same in both cases.

Comparison of core loss in BC choke and core loss of TLBC choke is shown in Fig. 12. In the figure p_{loss} is core loss in BC, and p_{loss1}, p_{loss2} are core loss in TLBC for modes 1 and 2 accordingly. From the figure it is clear that the core loss of the TLBC is smaller than the core loss of BC.
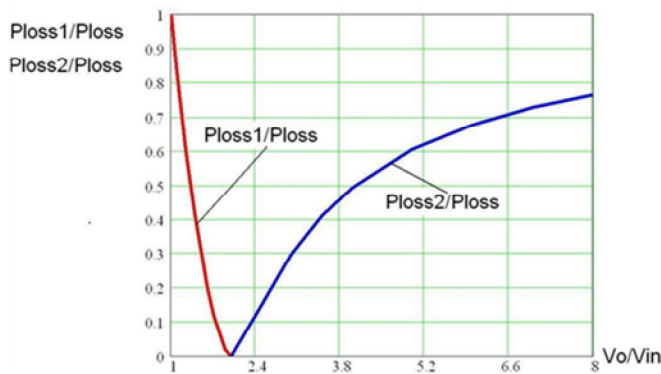

Figure 12. BC choke core loss versus of TLBC choke

C. Operation of power switches and diodes in TLBC

Analysis has shown that power loss in power switches and diodes in the TLBC for both modes are no more than in the BC. The reason of that is that lower voltage rated devices in TLBC have better conduction and switching characteristics than twice as much voltage rated devices in standard BC.

D. Capacitor operating conditions in TLBC and TLFCBC

One can ask the question: which topology, the TLBC or the TLFCBC is preferable? On the first view both topologies are equivalent: they use equal number of components, the same modes, with and without overlapping, the same TFR for continuous current of the choke. Nevertheless, there are substantial differences. The capacitors in TLFCBC have different voltage ratings, while the capacitors in TLBC have voltages equal to $V_o / 2$. Capacitor current ratings are also different for these topologies. Table 3 shows the ratio of RMS current values in capacitors to the load current for both circuits operating with and without overlapping.

TABLE III. EQUATIONS FOR CAPACITOR RMS CURRENT COMPARISON

Circuit	Mode	Capacitor	I_{rms} / I_{load}
TLBC	Without overlapping	C1 (C2)	$\sqrt{D/(2-D)}$
	With overlapping		$\sqrt{(1+D)/(1-D)}$
TLFCBC	Without overlapping	C1	$2\sqrt{D}/(2-D)$
	With overlapping		$2/\sqrt{1-D}$
	Without overlapping	C2	$\sqrt{D/(2-D)}$
	With overlapping		$\sqrt{(1+D)/(1-D)}$

Related plots based on equations in Table 3 are shown in Figs. 13 and 14.
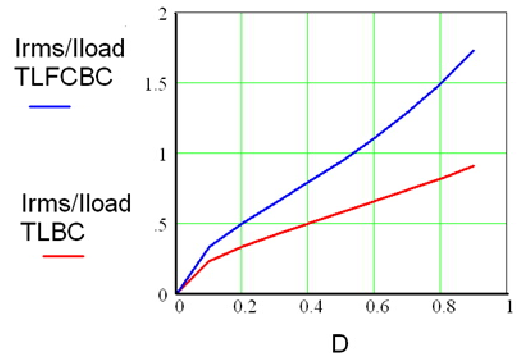

Figure 13. Relative RMS currents in capacitors of TLBC and TLFCBC operating without overlapping
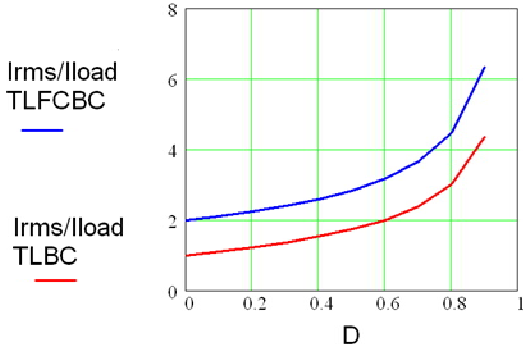
Figure 14. Relative RMS currents in capacitors of TLBC and TLFCBC operating in overlapping mode

VII. MULTILEVEL BOOST CONVERTERS

Four-level FCBC (FLFCBC) is shown in Fig.15 and four-level boost converter (FLBC) is shown in Fig. 16.
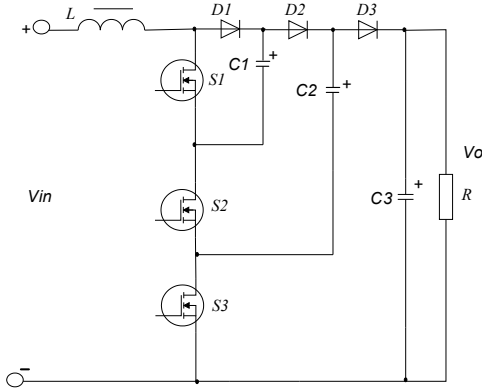

Figure 15. Four-level FCBC topology

For operation without overlapping, the control strategy in both topologies ensures that accumulation of energy in the choke occurs with voltages at capacitors subtracted from input voltage.
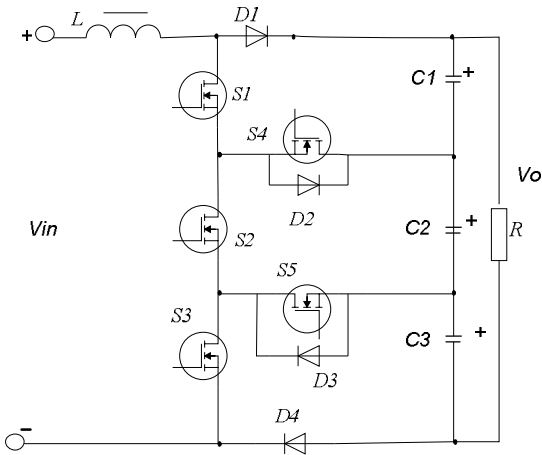

Figure 16. Four-level boost converter topology

For operation without overlapping, the control strategy in both topologies ensures that accumulation of energy in the choke occurs with voltages at capacitors subtracted from input voltage. Thus, in Fig. 15 accumulation occurs at V_{C1}, or at the difference between voltages V_{C1} and V_{C2}, or at the difference between voltages V_{C2} and V_{C3}. In Fig. 16 accumulation occurs only through one capacitor: $C1$, or $C2$, or $C3$. During pause interval, the energy is delivered to the output voltage. Having considered that a switching cycle of each transistor is T, and assuming that duty cycle D is $t_i/3$, for continuous current of the choke and operating without overlapping the following equation is applied for both topologies:

$$V_o = 3V_{in}/(3-2D). \qquad (12)$$

In operation with overlapping, the delivery of energy in the choke occurs for the lower voltage of the capacitors for both topologies. For continuous current of the choke and operating with overlapping for both topologies we have:

$$V_o = 3V_{in}/(1-D). \qquad (13)$$

In general, for any multilevel boost converters – MLFCBC or MLBC transfer function ratios are as following:

$$V_o = NV_{in}/(N-(N-1)D), \qquad (14)$$

and with overlapping:

$$V_o = NV_{in}/(1-D). \qquad (15)$$

In both last equations N is number of stages;

$D = t_i/(T/N)$;

T is switching cycle of one transistor.

The differences in capacitor operation for TLFCBC and TLBC topologies described earlier are applied to multilevel topologies as well: MLFCBC topologies require larger and more expensive capacitors compared with any MLBC.

The paper doesn't consider such important topic as asymmetry of capacitor operations for both topologies. The capacitor asymmetry could be the result of voltage deviation, caused by unequal heating of the switches, different parameters of the diodes etc. This topic and some others require a separate consideration.

VIII. EXPERIMENTAL RESULTS

Two laboratory prototypes of the TLBC were built for different requirements. The first prototype works at input voltages from 2200 V to 4000 V DC and provides an output power up to 90 kW at an output voltage of about 4300 V DC. This prototype operates in mode 1, i.e., without overlapping. The load of this converter is an unregulated resonant DC-DC converter. The output voltage of the DC-DC converter is regulated at 620V DC by PWM control of TLBC. The output voltage of the TLBC converter during the start-up is shown in Fig. 17.
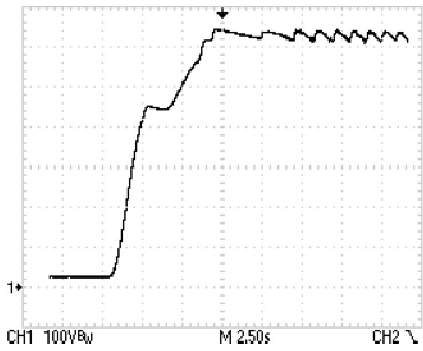
Figure 17. TLBC start-up waveform

Note, that the steady-state value of that output voltage is 620 V. The waveform was captured at Vin = 3300 V and without load.

Figure 18 shows the transient at the output of DC-DC converter after a step load change from no load to 90 kW. The efficiency of the whole design including the TLBC, the DC-DC converter followed by 3-phase inverters is 91%.
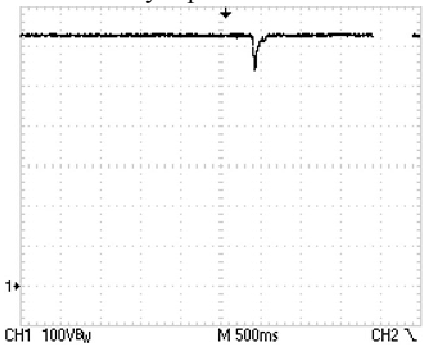

Figure 18. Transient at the output of DC-DC converter

The second prototype works at input voltages from 50 to 150 V DC. The TLBC section has the output voltage 400 V DC, the output power 3 kW and operates in mode 2 (with overlapping). The load is a three-phase inverter with frequency control for an asynchronous machine. Figure 19 shows the start-up process with input voltage 100 V.
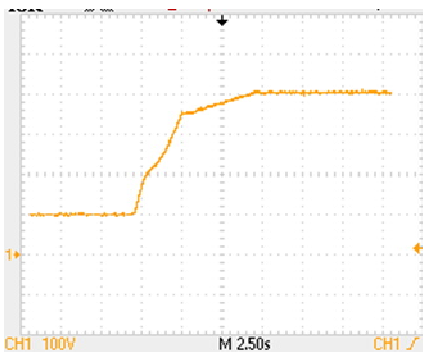

Figure 19. TLBC start-up in mode 2

Fig. 20 shows efficiency as a function of the input voltage with various output loads. The efficiency of the conventional boost converter under these conditions was lower by 1 to 3%.
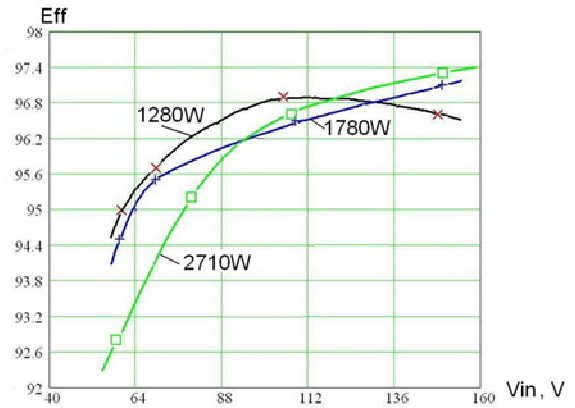

Figure 20. TLBC efficiency in mode 2

Fig. 21 shows the breadboard of the TLBC operating in mode 2 and 3-phase inverter.

Figure 21. TLBC breadboard with three-phase inverter at output, Po = 3 kW

The control systems of both designs were based on a DSP TMS320F2808. Each DSP provides PWM control of switches, generates protection signals based on data from comparators and sensors, controls the RS-485 interface and signal indicators. The DSP also monitors the current state of the system, and provides various test and service modes via a link with a computer.

IX.   CONCLUSION

The paper provides brief review of boost topologies described in literature and then focuses on their applications, specifically in renewable energy generation and transportation. Multilevel boost converters allow achieve high efficiency and power density by using lower voltage rated components. These converters require optimal drive and control technique and efficient power devices to demonstrate their full benefits. The review of emerging wide bandgap power devices and their optimal drive and control technique is outlined.

The steady state transfer function analysis at different modes of the operation for three-level and multilevel converters with flying capacitors and clamped diodes is

provided. Analysis also compares capacitor voltage and current rating and concludes that MLBC topology with clamped diodes has advantages versus MLFCC converter with flying capacitors. It is also shown that both MLBC and MLFCC boost topologies have advantages at high output voltage versus standard boost converter. It was demonstrated that the choke size and loss of TLBC converter are smaller than in standard boost converter. The experimental results of two breadboards 3kW and 90kW are provided including start up and efficiency to validate the analysis.

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