Digital Power Factor Correction. Recent approaches with and without current sensor

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***Abstract*— The impact of digital signal processing techniques applied to the design of controllers for power factor correction stages is reviewed. The analyzed contributions are oriented to eliminate or simplify the circuits that acquire and filter the converter variables as well as to improve the noise immunity and dynamic response. They are classified into two groups. The first group includes a current sensor. The second group faces the elimination of the current sensor for operation in continuous conduction mode, thus the duty cycle is defined by inaccurate estimation algorithms that limit the scope of application in which acceptable power factor is achieved. The paper puts especial emphasis on the latest authors´ original proposals that result in a universal controller, i.e. with no input voltage amplitude or frequency nor load limitations as long as the converter operates mostly in continuous conduction mode. The final aim is to specify a digital controller to be integrated in a field programmable gate array or in a specific circuit. Experimental results are presented as a proof of concept of the proposal.**

I. INTRODUCTION

Advanced digital control techniques for power converters, including power factor correction (PFC) rectifiers [1] have been presented in the recent years, some relevant examples are the following:

- Autotuning controllers set the desired crossover frequency and phase margin for the control loop by adjusting the compensator gain [2] or the PID parameters [3-4].
- Predictive current control: [5–9].
- Feedforward control to increase the crossover frequency of the current loop [9–12].
- Dynamic improvements: a) with Lyapunov-based digital control [13], b) with the utilization of the circle criterion [14], c) by modifying the output voltage ripple [15], d) by simply varying the gain of the voltage feedback loop considering the load variations [16], e) by replacing the energy storage capacitor (in 2-stage single-phase rectifiers) f) by a non-symmetric capacitive divider with independent voltage controls [17], or g) by using "dead-zone" digital controllers [18].
- Operation improvements over wide load ranges [19–23], or universal input voltage range [24].
- Control of interleaved or dual PFC converters: [25–29].
- Control of Bridgeless PFC Boost converters: [22, 30]

In [31] a digital implementation of a "nonlinear carrier" (NLC) control is presented in comparison with two different linear PFC controllers. Simulation and experimental results show a better behavior of the nonlinear controller in steady state (lower THDi and 3th current harmonic).

An interesting tendency is to avoid some measurements in the PFC stage. For example, in [6, 32–34] the input voltage is not measured, while in [35] the output voltage is the avoided measurement.

The concept of Harmonic Resistance in a Boost PFC converter with digital control is presented in [36].

Important aspects to take into account in digital controllers are the resources of the digital device, quantization effects and the clock frequency, which limit the switching frequency and introduce delays. Some works present algorithms with low requirements for the digital device [37, 38].

This work is organized as follows: Section II reviews contributions for PFC controllers that include an input current sensor. Section III presents realizations in which the current sensor is eliminated. Section IV presents experimental results of the authors' contributions on current sensorless PFC controllers, finalizing with conclusions.

II. DIGITAL POWER FACTOR CORRECTION CONTROLLERS WITH CURRENT SENSOR

Average Current Mode (ACM), has been the most prevalent analog solutions for CCM PFC rectifiers, being [39, 40] some examples of a digital implementation of the ACM relying on multiple current samples every switching period.

The capabilities of the digital devices are well suited for the implementation of nonlinear controllers. Digital signal processing enables the reduction of sensed variables and the design of more specific algorithms to improve the dynamic response and noise immunity. Illustrative examples can be found in [4, 18], where samples are avoided in the switch transition to prevent the effect of the switching noise in the control circuit or in [6], where the controller requires the sampling of two variables: the output voltage and the average input current; the input voltage being estimated. Leveraging the capabilities of the digital circuits, the average value of the sensed current is acquired from the MOSFET terminals synchronizing sampling and modulation, so that the current is always sampled in the middle of the ON-time and no low pass filter is used to acquire the mean value in each switching period. The current control is performed in this case with a dead-beat controller. A modification of this technique is

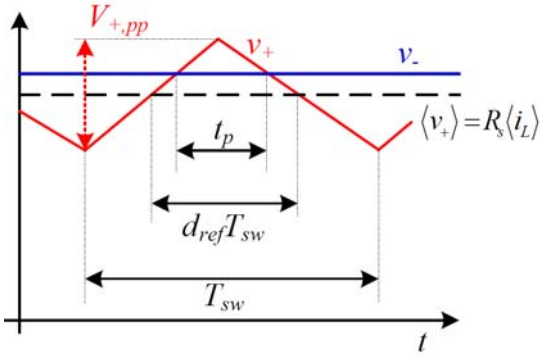


Figure 2. Operating waveforms of the average current sensor.

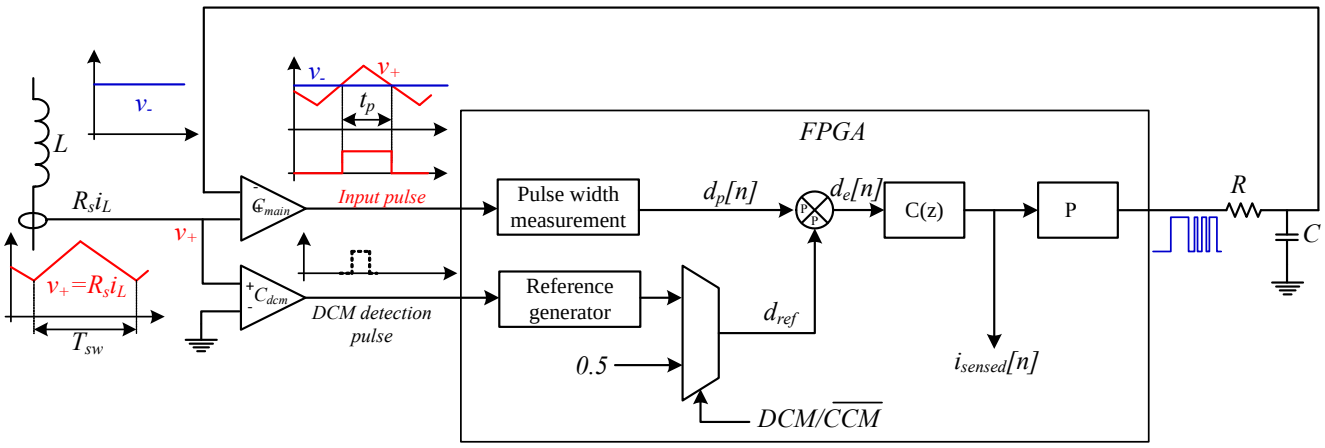


Fig. 1. Average current sensor scheme.

introduced in [32], where both variables, the input current and the output voltage, are acquired from the MOSFET terminals. The output voltage is measured with a small time delay after the turn-off event, and synchronized with the line voltage peak, rejecting the low-frequency output voltage ripple.

In [34] the current controller is a digital nonlinear carrier (DNLC) PFC controller, based on a simple control law which enables the CCM operation without input voltage sensing or estimation, becoming an US Patent in 2012 [41]. The current is sampled in the middle of the ON-time or also the OFF-time, and it uses a single comparator for the output voltage sensing [42].

Improvements in the output voltage dynamics are presented too in [43] where the output voltage sensor is replaced by a voltage estimation algorithm, with inherent cancellation of feedback voltage ripple. The current through the diode is used in [44] to compute the duty cycle without input voltage sensing.

The use of a feedforward control to improve the response of the current loop is introduced in [10], and digitally autotuning controllers are achieved by perturbing the PFC current and voltage loops [45].

A sampling algorithm for digitally controlled Boost PFC converters is presented in [46]. This algorithm, called "alternating-edge-sampling" (AES) presents switching noise immunity, straightforwardness, accurate measurement of the average input current, and the need for only few processor cycles.

One of the most recent works about low cost current sensors for PFC converters is [47], where no specific ADC IC is used. The analog-to-digital conversion is carried out with the concepts presented in [48-51]. The architecture of the proposed current sensor is shown in Fig. 1.

The instantaneous voltage of the current sensor is represented by $v_+ = R_s i_L$ and it is compared with two signals: One of these is the signal v_- which is compared by the comparator C_{main} whose output is called "*Input pulse*". The signal v_- represents the analog value of the digital current data $i_{sensed}[n]$ (output data of the sensor) which in steady state represents the average value of $\langle v_+ \rangle = R_s \langle i_L \rangle$. In the

comparator C_{dcm}, the signal v_+ is compared with 0 V. The signal *Input pulse* has a pulse duration t_p, and then a duty cycle $d_p = t_p/T_{sw}$, which is measured in the digital device $d_p[n]$. With the feedback operation and the controller $C(z)$, $d_p[n]$ is forced to be equal to d_{ref}. The reference signal d_{ref} is chosen depending upon the converter operation mode (for instance, if the converter operates in CCM then $d = 0.5$).

The waveforms of the average current sensor presented in [47] are shown in Fig. 2. The goal of the controllers is to match the signal v_- with the real average value of the current sample $\langle v_+ \rangle = R_s \langle i_L \rangle$. With that, it is obtained:

$$\langle d_p \rangle = \frac{t_p}{T_{sw}} = d_{ref} + \frac{\langle v_+ \rangle - v_-}{V_{+,pp}} \quad (1)$$

being $V_{+,pp}$ the current sample ripple amplitude. The block represented by "*Pulse-Width Measurement*" in Fig. 1 turns the output pulse duty cycle d_p into the digital signal $d_p[n]$.

The error signal $d_e[n]$, generated by the subtraction of d_{ref} from $d_p[n]$, is the input of the loop compensator $C(z)$. The output of the compensator $i_{sensed}[n]$ is turned back by a digital-to-analog converter formed by a Σ–Δ modulator and a RC low pass filter. The signal generated by the Σ–Δ modulator is a bitstream whose average values is equal to the $i_{sensed}[n]$ input signal.

The same approach is used to obtain the input and output voltage data, without $C(z)$ block and d_{ref} reference [52]. So, with this proposal, in [47] the analog-to-digital conversion of the three variables (input voltage, input current and output voltage) is carried out without any discrete ADC chip, being an inexpensive solution. The main drawback of this approach is that the current sensor has a bandwidth limited by the compensator $C(z)$, which in turns limits the bandwidth of the current loop.

Another one recent solution of a PFC CCM rectifier controller without any type of ADC chip is presented in [53], based on [49, 51]. The zero-crossings of the line voltage are detected by an isolated transformer and a zero crossing detector. The inductor current in sensed with a Hall sensor and the output voltage by a voltage divider, followed both by the sampling circuits presented in [53] to obtain the digital data of each variable. The sampling circuits are based on comparisons between the signals to be sampled and sawtooth waves, implemented with digital counters which count the duty cycle of these comparisons. The sinusoidal current command is generated by the zero-crossing detector and a sinusoidal look-up table.

III. Digital Power Factor Correction Controllers Without Current Sensor

The input current acquisition circuit usually represents a high cost; it may cause high local power losses (hot spot) in the resistive sensor and introduces switching noise along with gain compensation requirements in the control circuit. All of this motivates the research oriented to eliminate the current sensing.

In [54] the inductor current sensor is avoided, and it is replaced by a low speed load current measurement. One of the first works about PFC rectifiers without any current sensor is [55] where the duty cycle command is a function of the input and output voltages, the error between the output voltage and the reference voltage and $d|\sin\theta|/d\theta = \cos\theta$, where θ represents the phase angle of the input voltage v_g. In continuous conduction mode (CCM) Boost PFC Controllers, the most recent works proposing current sensorless solutions are [56,–61].

In [56], only the AC line voltage is detected and used to generate the switching signal for the MOSFET. So, not only the DC output voltage sensor but also the AC current sensor can be removed in the control system, respectively. A Kalman filter approach to estimate the input current is presented in [58]. Several works presented by Hung-Chi Chen avoid the current loop using the Single-Loop Current Sensorless Control (SLCSC) for single-phase boost-type PFC rectifier. This controller is firstly presented in [59] as the Duty Phase Control (DPC) and presented as SLCSC in [57], where the duty cycle command is computed taking into consideration the parasitic elements. Its model and small-signal Analysis is presented in [60]. This controller is designed taking into account the parasitic elements which are considered constants. It results in a good behavior under sinusoidal input voltages. A modification of the controller is presented in [61], where the input voltage is measured and the SLCSC is extended to work under distorted input voltages.

The idea of achieving power factor correction with a pre-calculated duty cycle for a line period in nominal conditions, and start applying these preprogrammed values at the half-line zero crossings is applied in [62–66]. In [62] no input voltage changes are considered, and the control responds to load changes. A predictive duty-cycle is presented in [63], with an implementation in a DSP, where the duty cycle command of the next AC line period is computed from the measurement of the input and output voltages. This solution presents limitations under load changes and it is improved in [64] with the measurement of the input current.

The pre-calculated duty-cycle technique strategy is applied in [65] with no current acquisition.

In [66], the control method is based on the experimental acquisitions of the duty-cycle command for different load conditions using a current sensor. These experimental acquisitions are programmed in the digital device and used to control the converter without the need of current sensor.

All the sensorless controllers mentioned previously achieve high power factor and low THD of the input current within the voltage and power ranges presented for each reference in Fig. 3 (according to the experimental results presented in each work).

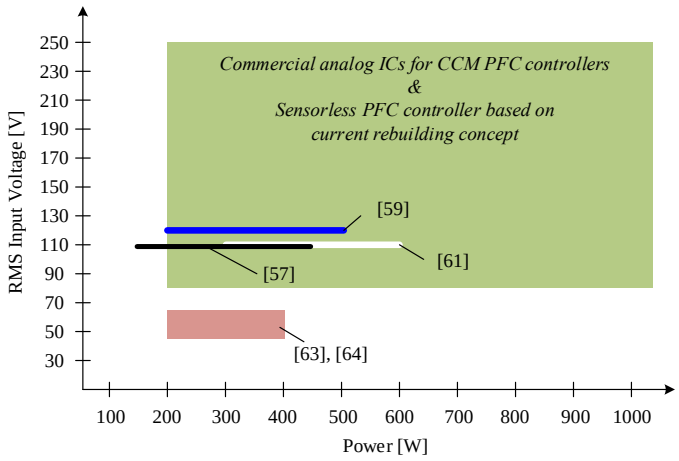


Fig. 3. Input voltage and power range of the recent works in sensorless PFC controllers.

In Fig. 3, the green area represents the target application range for the PFC controller without current sensor based on the digital estimation of the input current [52], [67-70], which cover the typical range of the commercial ICs [71] for CCM PFC controllers (universal input voltage range and wide output power range). In this controller, the input current measurement is substituted by the digital estimation of the current from the input and output voltage data. The variable volt-seconds (vs_L) across the inductor is computed in each switching period, and the small error (current estimation error) accumulated per switching period over the half line cycle is compensated.

The effect of the switching delays and a feedforward compensation technique is presented in [52].

The aim of the extra controller presented in [70] is to include a high resolution feedback control to automatically compensate for the current estimation error.

With this controller, a universal digital controller for Boost CCM power factor correction stages based on rebuilding concept is achieved. The term “universal” is used because with the extra fine feedback loop, the digital controller compensates for the estimation error, which is sensitive to the input voltage specifications and power conversion rate.

The feedback error compensation strategy is founded in the modeling of the influence of the different sources of current estimation error, such as the parasitic elements and errors in the voltage acquisition data. This accumulated error leads to typical current waveforms as the presented in Fig. 4. The digitally rebuilt input current i_{reb} is the variable used in the current loop (i.e. resulting sinusoidal), and the real current i_g, has a distortion due to this current estimation error i_{error}. The distortion causes a mismatch between the DCM times of both currents over the half line cycle. These times are labeled as T^{g}_{DCM} for the real current, and T^{reb}_{DCM} for the rebuilt current. Therefore, the digital controller extends its operation range in comparison with the previously presented solutions in sensorless Boost CCM PFC controllers. The behavior under different input voltage frequencies is also verified, showing a low THDi despite not measure the current.

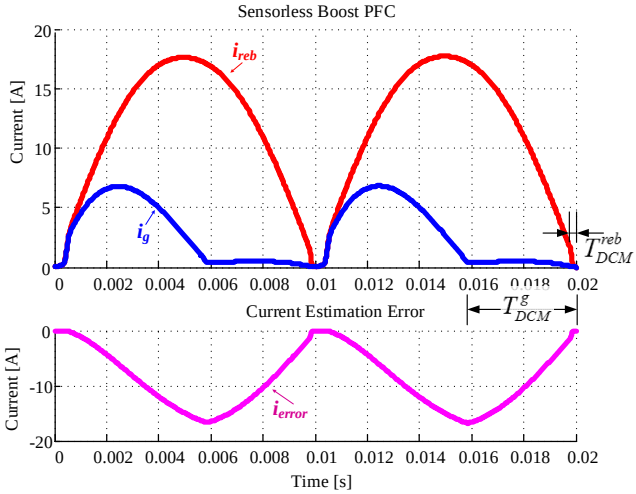


Fig.4. Current waveforms under a current estimation error situation.

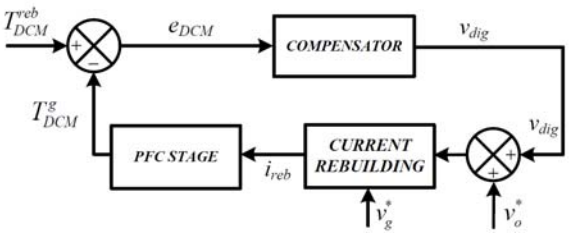


Fig. 5. Block diagram of the DCM time compensation controller.

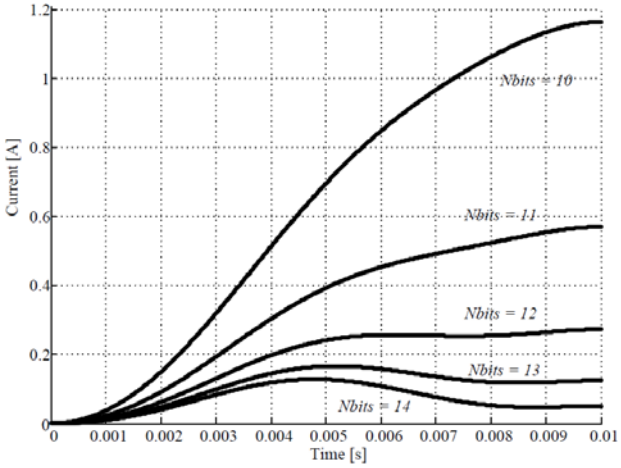


Fig. 6. Current estimation error resolution for different bits of resolution v_{dig}

A distortion in i_g leads to $T^{reb}_{DCM} \neq T^{g}_{DCM}$ reducing the power factor value. The digital controller captures these DCM times as is presented in [68, 69] and, measures and compares T^{g}_{DCM} and T^{reb}_{DCM} . DCM time error e_{DCM}, is defined by:

$$e_{DCM} = T^{reb}_{DCM} - T^{g}_{DCM} \quad (2)$$

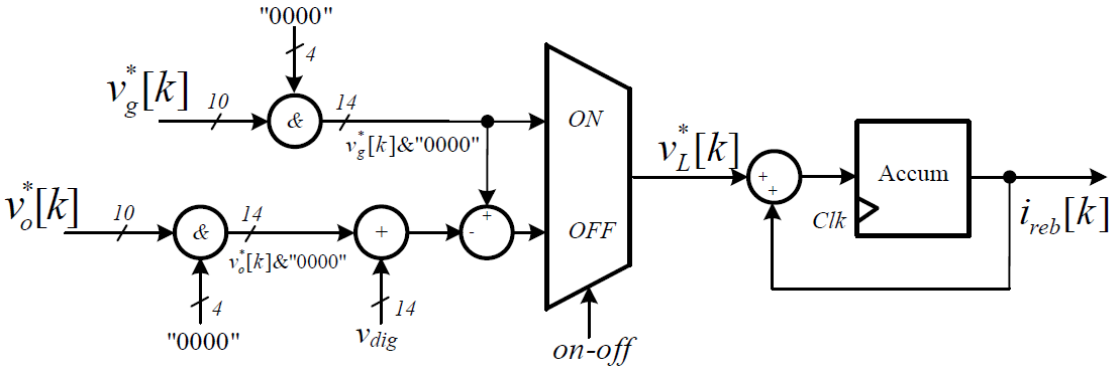


Fig. 7. Current estimator hardware implementation with higher resolution.

Thus, an indirect measurement of the current estimation error is obtained by e_{DCM}. The feedback loop adjusts a digital signal, labeled as v_{dig} to match $T_{DCM}^{reb} = T_{DCM}^{g}$. A block diagram of the proposed control loop is presented in Fig. 5. The DCM time error e_{DCM} is the input of an integral compensator, which adjust internally the value of the signal v_{dig} until the DCM times match, i.e. $e_{DCM} = 0$

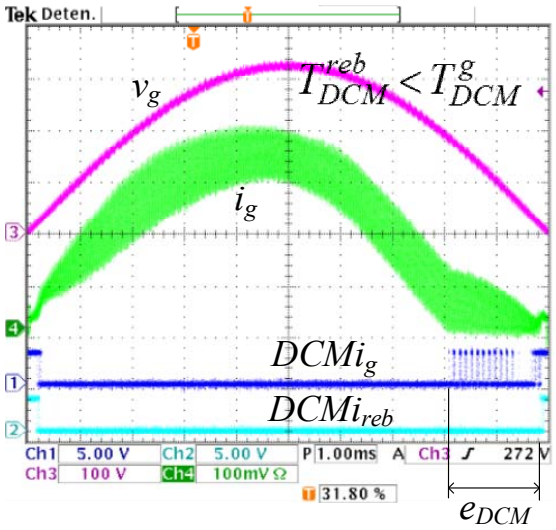
This feedback loop, modeled in [70], achieves the universality of the digital controller for sensorless Boost CCM power factor correction stages based on current rebuilding concept.

In a PFC operating in CCM, the DCM condition appears around the AC line zero crossings, where the duty cycle is ideally $d = 1$, but in the real implementation d is saturated before it reaches the unity. Therefore, under d saturation condition, T_{DCM}^{reb} is constant at different power levels, and is used as the DCM time reference. The compensator modifies the value of v_{dig} used in the digital current estimator. With the i_{reb} value, the duty cycle command is obtained and applied to the power stage.

The aim of this compensation technique is that the resolution of the v_{dig} signal can be incremented by the digital device, so with this v_{dig} signal all current estimation errors are compensated. However, v_{dig} has a finite resolution, so the digital controller sets a value $v_{dig} = V_{dig} \pm 0.5$ LSB (V_{dig} is the value in steady state). This 1 LSB uncertainty in v_{dig} represents a current estimation error i_{error}, over the half line cycle. This error is plotted in Fig. 6, for given the boost converter parameters. This compensation can be implemented with a resolution in the current estimation error higher than the feedforward compensation, whose resolution is limited by the digital device clock period (that results in a current estimation error at the end of the half line cycle up to ± 2 A).

Figure 7 represents the following real case: A 10-bit ADC is used for the input and output voltages ($v_g^*[k]$ and $v_o^*[k]$), and 4 LSBs are concatenated to obtain a 14 bits length. The signal v_{dig} are 14-bits length data to have the resolution required in the system, and is added to $v_o^*[k]$. With this approach, the resolution can be increased as needed by adding more LSBs to v_{dig},. The signal v_{dig} is function of the power converted and the current estimation error, which creates a difference between the DCM time of i_{reb}, and the DCM of i_g over the half line cycle. Therefore, these DCM times are used in the new proposed feedback loop to set v_{dig} in steady state.

As a real example, Fig. 8 shows two compensation situations for different values of v_{dig} when current estimation error exists. If $e_{DCM} < 0$ then $i_{reb} > i_g$, so it is necessary to increase v_{dig}, and then decrease i_{reb} to match the DCM times of the input and rebuilt input current. On the other hand, if $e_{DCM} > 0$ then $i_{reb} < i_g$, being necessary to decrease v_{dig} to increase i_{reb}.



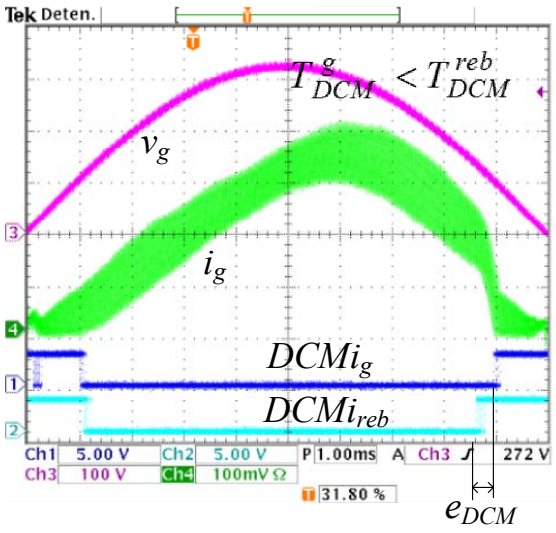


Fig. 8. Real waveforms. Input voltage v_g, real input current i_g, waveforms and digital for the cases: above $e_{DCM} < 0$ and below $e_{DCM} > 0$

IV. Experimental results

A 1 kW boost converter with the proposed digital feed forward and feedback loops has been built and tested. The output voltage reference is 400 V_{dc} with an input voltage ranging from 120 V_{rms} to 250 V_{rms}. The switching frequency is 96 kHz. The output capacitor $C = 220\ uF$, an inductor of 1 mH, the MOSFET and diode used to build the prototype were a IRFP27N60K from International Rectified ™ a IDH12S60 from Infineon ™ The digital PFC controller is described in VHDL and implemented on a XC3S200E field programmable gate array (FPGA) of Xilinx. A second order *ad-hoc* sigma delta ADC is used for the output voltage and a commercial TLV1572 serial 10-bit ADC for the input voltage to obtain the voltage data

The DCM time feedback loop sets v_{dig} to compensate the current estimation error in all the different situations. To evaluate this approach, the converter controlled by the FPGA has been tested under different voltage, grid frequency, and load steps randomly applied. The results of this experiment are presented in Fig. 9. The variables V_g (RMS input voltage)

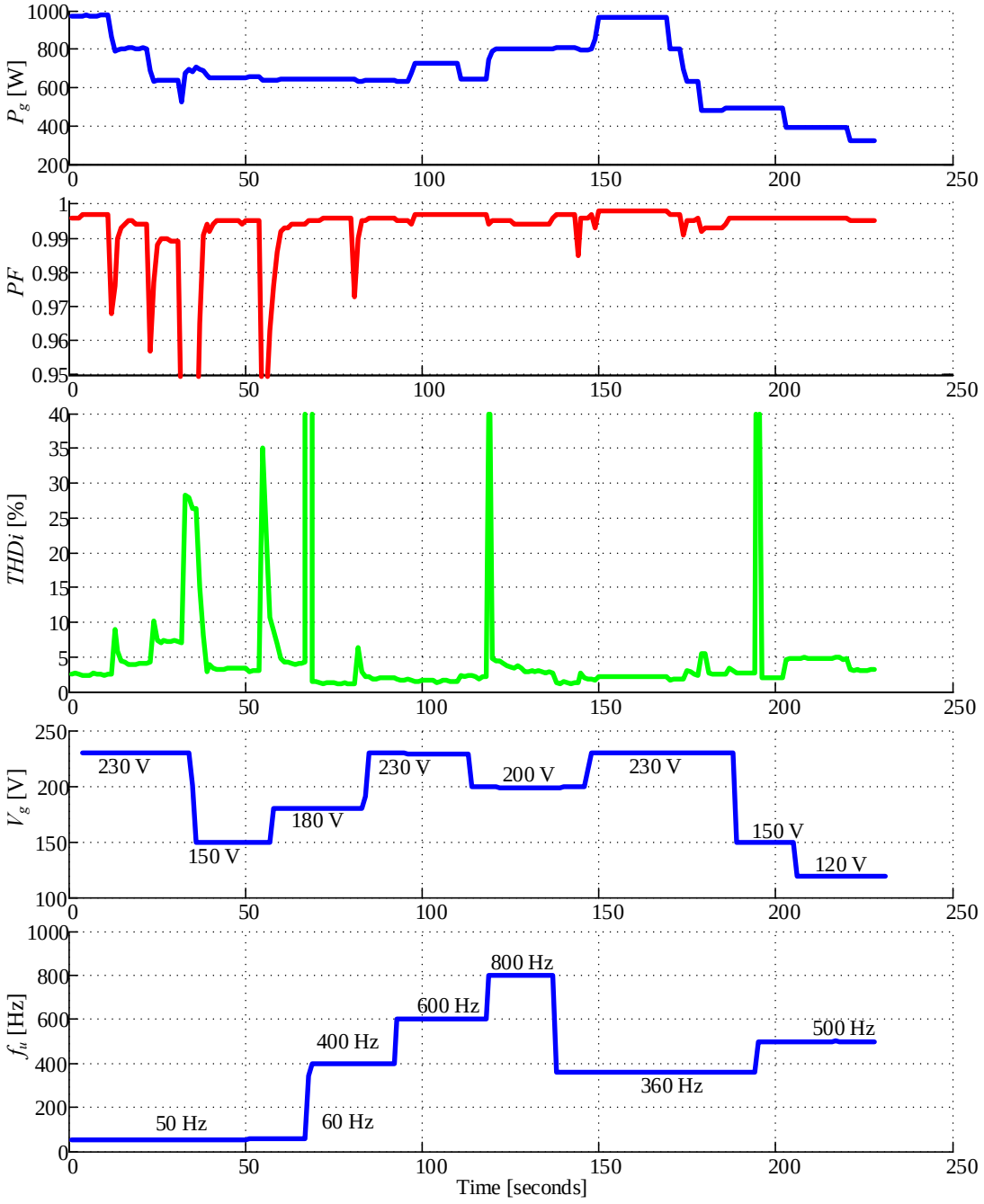


Fig. 9. Time evolution of the different electrical variables with $V_o = 400V_{dc}$, $f_{sw} = 96$ kHz

and f_u (grid frequency) are modified manually in the 6813B AC power source of Agilent, used to supply the boost converter, and the power demanded from the grid P_g (input voltage) is changed with load steps. *PF* (power factor) and *THDi* are the "output" variables used to evaluate the behavior of the controller. It can be observed how every step in V_g, f_u or P_g decreases the PF value. The more aggressive the step is the higher instantaneous change in the *PF* value occurs. At the same time, in parallel with the *PF* modification, the *THDi* value increases. This current distortion is detected by the DCM time feedback loop which compensates the DCM time mismatch, increasing the PF always with a higher value than 0.990. There are 3 points where the *THDi* looks like an impulse but the PF keeps high, those correspond with grid frequency steps-up in which the measurement given by the power analyzer is no correct.

The current and voltage waveforms under 50 and 60 Hz of them are presented in Fig. 10 and 11, respectively. Figure 10 corresponds with the measurements done at V_g =229 V, f_u =50 Hz, *THDi* =1.88 %, *PF* = 0.999, P_g =964.6 W. Figure 11 corresponds with V_g =119 V, f_u =60 Hz, *THDi* =2.15 %, PF =0.998, P_g =491.3 W.

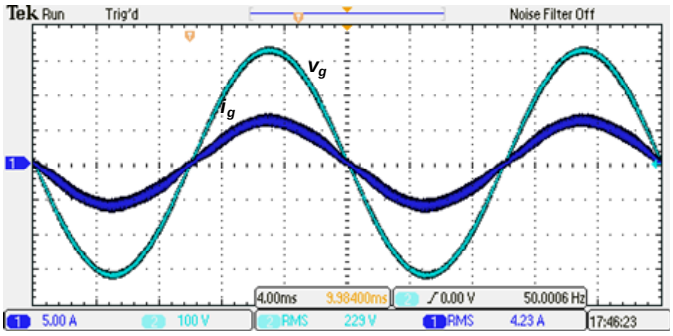


Fig. 10. Experimental results. V_g =229 V, f_u =50 Hz, *THDi* =1.88 %, *PF* =0.999, P_g =964.6 W

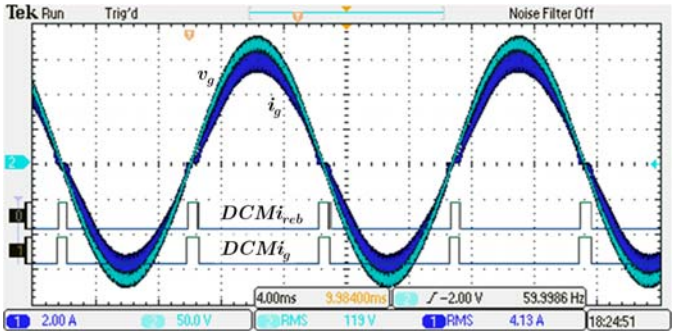


Fig. 21. Experimental results. V_g =119 V, f_u =60 Hz, *THDi* =2.15 %, *PF* =0.998, P_g =491.3 W

V. Conclusions

A review of the digital circuit proposal to design controllers for PFC stages has been presented. In addition to the advantages that the digital controllers obtain for power converters in terms of flexibility and synchronization, PFC stages benefit from simplifications in the power variables acquisition circuits and filters, resulting in cost savings and better power efficiency and lower harmonic distortion.

The application range of PFC controllers that eliminate the current sensor covers all the input voltage amplitudes and frequencies as well as a wide load range when a complete cancelation of the current estimation errors is achieved with an extra feedback loop is included to this purpose.

The proposed sensorless PFC controller for Boost rectifiers based on current rebuilding concept is "universal" because the controller does not require to be tuned for a given power or voltage range and extends the operation range in comparison with the previous solutions presented in sensorless Boost CCM PFC controllers. This specific feedback loop is inherently slow and obtains the duty cycle with the required resolution. The PFC response is improved with predictive modulators and feed forward algorithms that rapidly approach the duty cycle sequence to the optimum. From the experimental results it can be concluded that the best PF and THDi are obtained at the highest power levels. Anyhow and in all the tested conditions, the harmonic content is well below the limits given by the strictest standards. It must be remarked that the digital controller has not been re-tuned or modified to operate under the different conditions, showing the universality of the presented approach

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