Three-Level Neutral-Point-Clamped Quasi-Z-Source Inverter as a New Solution for Renewable Energy Application

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Abstract—**This paper describes the new three-level neutral-point-clamped quasi-z-source inverter. Using results of continuous current mode analysis as well as efficiency and voltage quality comparative evaluations, the new modulation technique for this converter was proposed. This modulation technique uses special modified shoot-through mode in output inverter stage to realize the adjustment of boost factor for maximum power point tracking. The control system was built on FPGA, that allows to implement plenty evaluation and control functions in one chip. All proposed solutions were verified by different simulations in PSCAD and MATLAB Simulink. The experimental prototype was built and the results of experimental investigations in laboratory conditions are presented.**

I. Introduction

In recent years three-level inverters have received increasing attention in industrial applications, such as motor drives [1], [2], active filters [3], [4] and renewable energy systems [5]. Compared to the traditional two-level voltage source inverters, the major advantage of multilevel inverters is the stepwise output voltage [1]-[6]. This advantage results in higher power quality, higher voltage capability, better electromagnetic compatibility, lower switching losses, and needlessness of a transformer at distribution voltage level [6], [7].

In contrast to the two-level voltage source inverter, the three-level neutral-point-clamped (3L-NPC) inverter has many advantages, such as lower semiconductor voltage stress, lower required blocking voltage capability, decreased *dv/dt*, better harmonic performance, soft switching possibilities without additional components, higher switching frequency due to lower switching losses, and balanced neutral-point voltage. However, as a drawback, it has two additional clamping diodes per phase-leg and more controlled semiconductor switches per phase-leg than the two-level voltage source inverter (VSI). The 3L-NPC can normally perform only the voltage buck operation. The ac output voltage is limited below and cannot exceed the DC-link voltage or the DC-link voltage has to be higher than the AC output voltage. The shoot-through problem caused by EMI noise's mis-gating-on is a major killer to the converter's reliability. Dead-time to block both upper and lower devices has to be provided in the VSI, which causes waveform distortion.

In order to ensure voltage boost operation an additional DC/DC boost converter should be used in the input stage. At the same time, the Z-source inverter (ZSI) has been proposed in [8] to overcome the limitations and problems of the traditional VSI and the current-source inverter (CSI). Such topology provides boost function with shoot-through immunity that is not forbidden [9], [10].

In the paper [11] the combination of three-level neutral-point-clamped topology with a Z-source network is presented. Proposed topology combines advantages of the three-level inverter with the Z-source network. The main drawback of the proposed scheme is its separated voltage source.

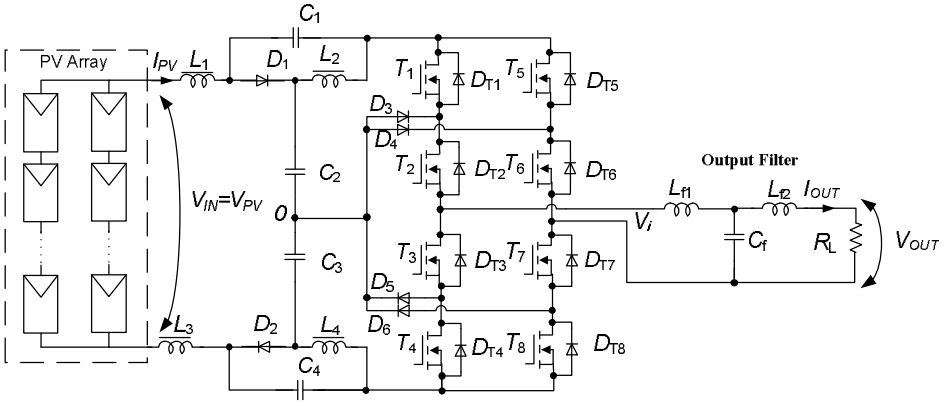


Fig. 1. 3L-NPC qZSI topology.

The quasi-Z-source inverters (qZSIs) have been proposed in [12]-[14] to further improve on the traditional ZSIs. Besides the advantages inherited from the ZSIs, the qZSIs also have several of their own merits, such as reduced passive component ratings, continuous input current configuration, a common dc rail between the source and the inverter. qZSIs suit very well for renewable energy systems [14]-[21] because of excellent performance and availability of all the requirements for PV systems. These inverters are capable of performing maximum power point tracking (MPPT) and inversion with no need for extra DC/DC converter. At the same time, continuous input current makes it especially suitable for fuel cell applications [14]. A three-level neutral-point-clamped quasi-Z-source inverter (3L-NPC qZSI) proposed recently is a new modification of the qZSI [22], [23]. The new converter combines the advantages of the qZSI and NPC topologies described above.

Fig. 1 illustrates the proposed topology of a 3L-NPC qZSI. As advantages, this topology can have continuous input current, the possibility to use shoot-through, lower switching losses and balanced neutral-point voltage in comparison with the traditional two-level voltage source inverter. At the same time, the shoot-through switching state demands new approaches in the modulation technique to combine the boost factor with the best possible voltage quality.

As a result, such topology is suitable for photovoltaic applications because the boost capability and the shoot-through duty cycle allow compensating the influence of the irradiance and temperature changes on the input voltage and realize the MPPT algorithm.

This paper presents a detailed steady-state analysis of a single phase 3L-NPC qZSI in the case of the continuous conduction mode (CCM). CCM and discontinuous conduction mode (DCM) condition with design guidelines is described. Special new modulation technique with distributed shoot-through generation is discussed. Experimental results are given to verify the theoretical analysis.

II. General Description and Steady-State Analysis of 3L-NPC qZSI

Each leg of the 3L-NPC qZSI consists of two complementary switching pairs and four anti-parallel diodes (Fig. 1). Shoot-through states are equally distributed over the operating period of the inverter. The inverter output voltage has five different levels: 0, $\pm B\cdot(V_{IN}/2)$ and $\pm B\cdot V_{IN}$ in the positive and negative directions, where B is the inverter boost factor. The shoot-through vector is generated separately. Finally, the shoot-though vector is mixed with other control signals.

In general, the operating period of the 3L-NPC qZSI in the CCM may be divided into 8 time intervals. All the switching states can be separated into three main modes: zero state, active states and shoot-through state. On the other hand, active states are separated on the three submodes.

An equivalent scheme for zero-state intervals is shown in Fig. 2 *a*. Equations that describe the behavior of the converter in this mode are as follows:

$$V_{IN} - L_1\frac{dI_{L1}}{dt} - V_{C2} - V_{C3} - L_3\frac{dI_{L3}}{dt} = 0, \quad (1)$$

$$V_{C1} + L_2\frac{dI_{L2}}{dt} = 0, \quad (2)$$

$$L_4\frac{dI_{L4}}{dt} + V_{C4} = 0, \quad (3)$$

$$I_{L1} = I_{L3}, \quad (4)$$

$$I_{L1} + C_1\frac{dV_{C1}}{dt} - I_{L2} - C_2\frac{dV_{C2}}{dt} = 0, \quad (5)$$

$$C_3\frac{dV_{C3}}{dt} + I_{L4} - C_4\frac{dV_{C4}}{dt} - I_{L3} = 0, \quad (6)$$

$$C_2\frac{dV_{C2}}{dt} - C_3\frac{dV_{C3}}{dt} = 0, \quad (7)$$

$$V_{AB} = 0. \quad (8)$$

An equivalent scheme for the shoot-through intervals is shown in Fig. 2 *b*. Equations that describe the behavior in this mode are as follows:

$$V_{IN} - L_1\frac{dI_{L1}}{dt} + V_{C1} + V_{C4} - L_3\frac{dI_{L3}}{dt} = 0, \quad (9)$$

$$V_{C2} - L_2\frac{dI_{L2}}{dt} = 0, \quad (10)$$

$$V_{C3} - L_4\frac{dI_{L4}}{dt} = 0, \quad (11)$$

$$I_{L1} = I_{L3}, \quad (12)$$

$$I_{L1} + C_1\frac{dV_{C1}}{dt} = 0, \quad (13)$$

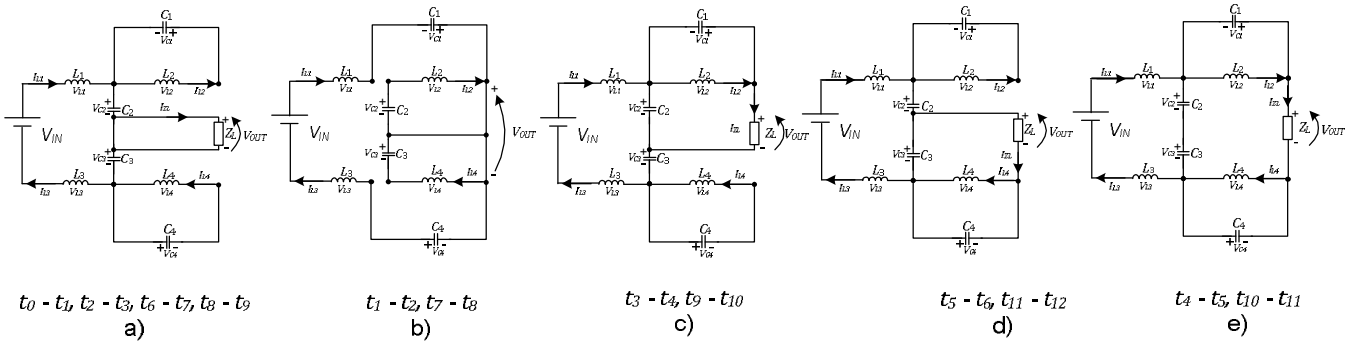


Fig. 2. Equivalent schemes of main operating modes.

$$C_3 \frac{dV_{C3}}{dt} + I_{L4} = 0 . \quad (14)$$

$$V_{AB} = 0 . \quad (15)$$

The first equivalent scheme for the active state is shown in Fig. 2 *c*. It corresponds to the case when the output voltage is equal to half the DC-link voltage. The middle point is clamped through the load to the high side of the DC-link. Equations (16) to (25) describe the behavior in this mode:

$$V_{IN} - L_1 \frac{dI_{L1}}{dt} - V_{C2} - V_{C3} - L_3 \frac{dI_{L3}}{dt} = 0 , \quad (16)$$

$$V_{C1} + L_2 \frac{dI_{L2}}{dt} = 0 , \quad (17)$$

$$L_4 \frac{dI_{L4}}{dt} + V_{C4} = 0 , \quad (18)$$

$$V_{C2} - L_2 \frac{dI_{L2}}{dt} - V_{AB} = 0 , \quad (19)$$

$$I_{L1} = I_{L3} , \quad (20)$$

$$I_{L1} + C_1 \frac{dV_{C1}}{dt} - I_{L2} - C_2 \frac{dV_{C2}}{dt} = 0 , \quad (21)$$

$$I_{L2} - C_1 \frac{dV_{C1}}{dt} - I_{ZL} = 0 , \quad (22)$$

$$C_3 \frac{dV_{C3}}{dt} + I_{L4} - C_4 \frac{dV_{C4}}{dt} - I_{L3} = 0 , \quad (23)$$

$$C_2 \frac{dV_{C2}}{dt} - C_3 \frac{dV_{C3}}{dt} + I_{ZL} = 0 , \quad (24)$$

$$V_{AB} = I_{ZL} Z_L . \quad (25)$$

The second equivalent scheme for the active state is shown in Fig. 2 *d*. It corresponds to the case when the output voltage is equal to half the DC-link voltage and the middle point is clamped through the load to the low side of the DC-link. Eqs. (26) to (35) describe the behavior in this mode:

$$V_{IN} - L_1 \frac{dI_{L1}}{dt} - V_{C2} - V_{C3} - L_3 \frac{dI_{L3}}{dt} = 0 , \quad (26)$$

$$V_{C1} + L_2 \frac{dI_{L2}}{dt} = 0 , \quad (27)$$

$$L_4 \frac{dI_{L4}}{dt} + V_{C4} = 0 , \quad (28)$$

$$V_{C3} - V_{OUT} - L_4 \frac{dI_{L4}}{dt} = 0 , \quad (29)$$

$$I_{L1} = I_{L3} , \quad (30)$$

$$I_{L1} + C_1 \frac{dV_{C1}}{dt} - I_{L2} - C_2 \frac{dV_{C2}}{dt} = 0 , \quad (31)$$

$$I_{ZL} - I_{L4} + C_4 \frac{dV_{C4}}{dt} = 0 , \quad (32)$$

$$C_3 \frac{dV_{C3}}{dt} + I_{L4} - C_4 \frac{dV_{C4}}{dt} - I_{L3} = 0 , \quad (33)$$

$$C_2 \frac{dV_{C2}}{dt} - C_3 \frac{dV_{C3}}{dt} - I_{ZL} = 0 , \quad (34)$$

$$V_{AB} = I_{ZL} Z_L . \quad (35)$$

The third equivalent scheme for the active state is shown in Fig. 2 *e*. It corresponds to the case when the output voltage is equal to the DC-link voltage. Eqs. (36) to (45) describe the behavior of the converter in this mode:

$$V_{IN} - L_1 \frac{dI_{L1}}{dt} - V_{C2} - V_{C3} - L_3 \frac{dI_{L3}}{dt} = 0 , \quad (36)$$

$$V_{C1} + L_2 \frac{dI_{L2}}{dt} = 0 , \quad (37)$$

$$L_4 \frac{dI_{L4}}{dt} + V_{C4} = 0 , \quad (38)$$

$$V_{C3} + V_{C2} - L_2 \frac{dI_{L2}}{dt} - V_{OUT} - L_4 \frac{dI_{L4}}{dt} = 0 , \quad (39)$$

$$I_{L1} = I_{L3} , \quad (40)$$

$$I_{L1} + C_1 \frac{dV_{C1}}{dt} - I_{L2} - C_2 \frac{dV_{C2}}{dt} = 0 , \quad (41)$$

$$I_{ZL} - I_{L4} + C_4 \frac{dV_{C4}}{dt} = 0 , \quad (42)$$

$$C_3 \frac{dV_{C3}}{dt} + I_{L4} - C_4 \frac{dV_{C4}}{dt} - I_{L3} = 0 , \quad (43)$$

$$I_{L2} - C_1 \frac{dV_{C1}}{dt} - I_{ZL} = 0 , \quad (44)$$

$$V_{AB} = I_{ZL} Z_L . \quad (45)$$

To simplify the analysis it was assumed that the input capacitors and inductors are identical, thus:

$$L_1 = L_3 , \quad L_2 = L_4 , \quad (46)$$

$$C_1 = C_4 , \quad C_2 = C_3 . \quad (47)$$

The operating period of the converter in the CCM could be represented as

$$\frac{t_N}{T} + \frac{t_S}{T} = D_N + D_S = 1 . \quad (48)$$

where D_N is the duty cycle of the non-shoot-through and D_S is the shoot-through duty cycle.

In the steady state, over one switching period the average voltage of the inductor over one switching period is zero and the voltages across the capacitors are constant. Thus, by Eqs. (1) to (45), the voltages across the capacitors can be found:

$$V_{C1} = V_{C4} = \frac{D_S \cdot V_{IN}}{2 - 4 \cdot D_S} , \quad (49)$$

$$V_{C2} = V_{C3} = \frac{V_{IN} \cdot (1 - D_S)}{2 - 4 \cdot D_S} . \quad (50)$$

The peak DC-link voltage is the sum of all the capacitor voltages:

$$V_{DC} = V_{C1} + V_{C2} + V_{C3} + V_{C4} = \frac{V_{IN}}{1 - 2 \cdot D_S} . \quad (51)$$

We can define the total boost factor as:

$$B = \frac{V_{OUT\_MAX}}{V_{IN}} = \frac{V_{DC} \cdot M}{V_{IN}} , \quad (52)$$

where M is the amplitude modulation index that taking into consideration the shoot-through intervals is limited to $M=1-Ds$, so the total boost factor will be

$$B = \frac{V_{OUT\_MAX}}{V_{IN}} = \frac{V_{DC} \cdot (1 - D_S)}{V_{IN}} = \frac{1 - D_S}{(1 - 2 \cdot D_S)} . \quad (53)$$

III. CCM Condition and Some Design Guidelines for the 3L-NPC qZSI

In an ideal case, the DC-link voltage and the input current of the 3L-NPC qZSI are constant [10], [24]. The main problem lies in the floating instantaneous power consumption that evokes current fluctuations in the corresponding capacitors. A simplified equivalent scheme of the qZS network is shown in Fig. 3 *a*. The capacitors and inductors are represented as ideal voltage and current sources, correspondingly. The idealized operating waveforms of the 3L-NPC qZSI are shown in Fig. 3 *b*.

In a real system, the operating waveforms are distorted by the ripple, as shown in Fig. 3 *c*. As can be seen, the DC-link voltage has low frequency fluctuation (100 Hz) caused by instantaneous output power. As a result, it causes low frequency input current fluctuations. Also, it should be noticed that the input current has high frequency ripple. It is connected with the high frequency shoot-through duty cycle switching.

In order to eliminate low frequency fluctuations in the system it is necessary to maintain constant voltages across the capacitors despite the AC component present in the DC-link current.

Capacitor voltage ripple can be expressed as

$$\Delta V_{C1} = \Delta V_{C4} = \frac{1}{C_1}\int_0^{T/4} i_C(t)dt = \\ = \frac{1}{C_1}\int_0^{T/4} \frac{P_{OUT}}{V_{DC}} \cdot sin(2 \cdot \frac{2\pi}{T} \cdot t)dt = \frac{T \cdot P_{OUT}}{2\pi \cdot C_1 \cdot V_{DC}}, \quad (54)$$

where T is the period of the sinusoidal output voltage.

The required value of the capacitance of C_1 to maintain the desired voltage ripple factor K_C can be obtained using Eqs. (49), (53) and (54):

$$K_C = \frac{\Delta V_{C1}}{V_{C1}} = \frac{T \cdot P_{OUT} \cdot (1-D_S)^2}{\pi \cdot C_1 \cdot V^2_{OUT\_MAX} \cdot D_S}, \quad (55)$$

where K_C is the voltage ripple factor, V_{OUT_MAX} is an amplitude value of the output voltage.

As a result, the capacitor can be calculated:

$$C_1 \geq \frac{T \cdot P_{OUT} \cdot (1-D_S)^2}{\pi \cdot K_C \cdot V^2_{OUT\_MAX} \cdot D_S}. \quad (56)$$

Capacitance values for capacitors C_2, C_3 could be defined similarly:

$$C_2 \geq \frac{T \cdot P_{OUT} \cdot (1-D_S)}{\pi \cdot K_C \cdot V^2_{OUT\_MAX} \cdot}. \quad (57)$$

A decrease in speed is defined by the equivalent schemes and it depends on the load resistance R. The rising speed depends on the inductor and capacitor voltages. It means that high frequency ripple of the current can be found from the shoot-through interval.

From Eq. (9) we obtain:

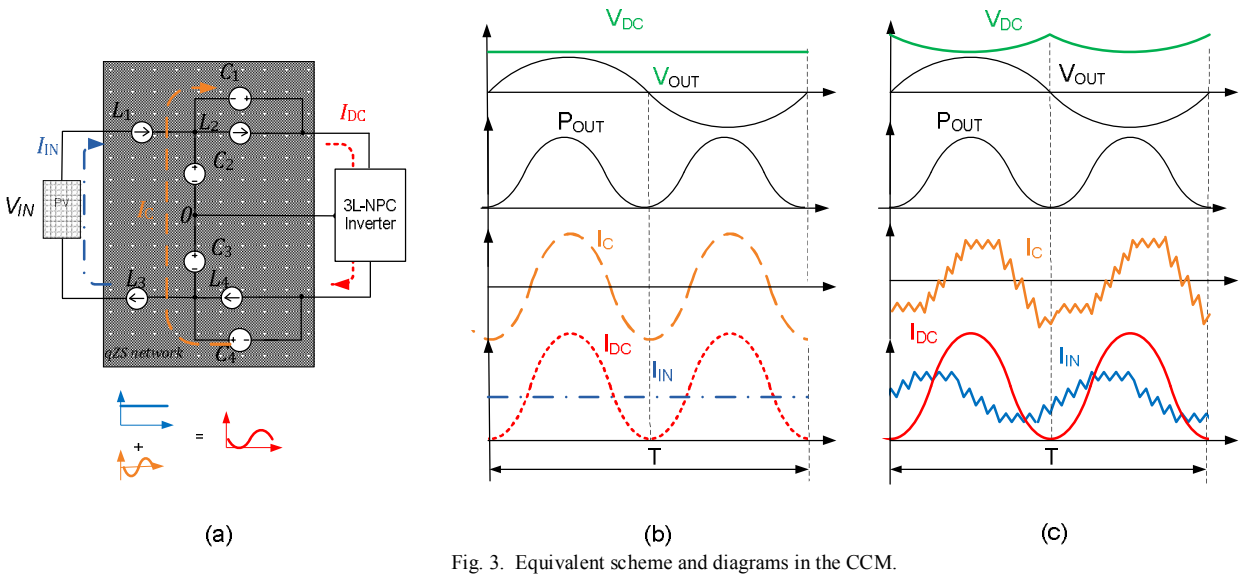
$$\Delta I_{L1} = \int_0^{T_S \cdot D_S} \frac{dI_{L1}}{dt} \cdot dt = \int_0^{T_S \cdot D_S} (\frac{V_{IN} + V_{C1} + V_{C4}}{2 \cdot L}) \cdot dt = \\ = (\frac{V_{IN} + V_{C1} + V_{C4}}{2 \cdot L}) \cdot T_S \cdot D_S, \quad (58)$$

where T_S is the switching period. In order to maintain the CCM operation of the converter the input current ripple ΔI_{L1} should be smaller than the average input current I_a. The average input current can be defined from the power balance:

$$P_{IN} = V_{IN} \cdot I_a = P_{OUT}. \quad (59)$$

Taking into account the CCM condition with predefine current ripple from Eqs. (49), (58) and (59) we can express:

$$K_L = \frac{\Delta I_{L1}}{I_a} = \frac{V^2{}_{OUT\_MAX} \cdot (1-2 \cdot D_S)}{2 \cdot (1-D_S) \cdot L \cdot P_{OUT}} T_S \cdot D_S, \quad (60)$$



(a) (b) (c)

Fig. 3. Equivalent scheme and diagrams in the CCM.

and finally we can express:

$$L \geq \frac{V^2_{OUT\_MAX} \cdot (1-2 \cdot D_S)}{2 \cdot (1-D_S) \cdot K_L \cdot P_{OUT}} T_S \cdot D_S . \quad (61)$$

It means that we can define the minimum value of the inductance in order to guaranteeing a ripple in the induction current and as a result to maintain the CCM operation of the proposed inverter.

IV. New Modulation Technique

There are several pulse width modulation (PWM) techniques that could be applied for the 3L-NPC qZSI [9], [25]-[27].The core idea of these methods is presented in Fig. 4. All of them generate the shoot-through states when the output voltage is in the zero state (V_{AB} = 0) in order to maintain constant and unaltered normalized average voltage per switching period whereas the shoot-through states are carefully and centrally added to the active states that enable the number of higher harmonics to be kept to a minimum.

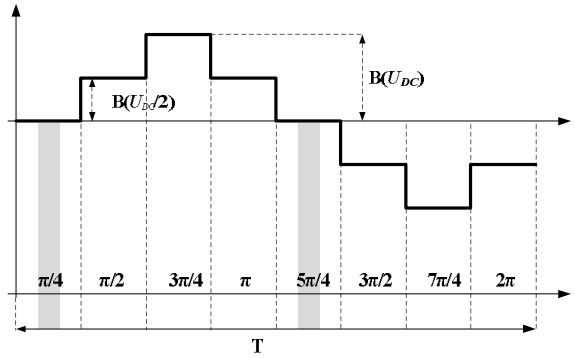


Fig. 4. Output voltage waveform of the traditional shoot-through PWM for the 3L-NPC qZSI.

Using these PWM techniques for the 3L-NPC qZSI, the V_{AB} has only two zero states per period and shoot-through states can only be placed during these two intervals ([0, π/4] and [π, 5π/4]).

These techniques present some problems, such as a larger size of the passive elements, more input current ripple and capacitor voltage disbalance.

A. Description of General Principles

Fig. 5 *a* shows a sketch of the proposed modulation technique.

One modulating sinusoidal wave and four triangular carriers are compared to obtain the different states of T_1, T_2, T_5 and T_6 and T_3, T_4, T_7 and T_8 have the complementary state of the other, respectively.

$Carrier_1$ is used to generate the shoot-through states in comparison with a constant value that includes the desired D_s value. Operating in this way, uniformly distributed shoot-through states with the constant width during the whole output voltage period can be achieved.

In order to compensate the average voltage V_{AB} when the shoot-through states are applied, leg *B* must compensate this situation through the change of the voltage V_{B0}. Fig. 5 *b* shows how we can obtain this compensation.

During the positive semi-cycle, leg *B* has to produce $U_{B0} = -V_{DC}/2$ more times to restore the average voltage U_{AB}. This is produced through $carrier_4$ displacement that generates the pulses of T_6. During the negative semi-cycle the same situation is produced. Leg *B* has to produce $V_{B0} = +V_{DC}/2$ more times to restore the average voltage V_{AB}. This is produced through $carrier_3$ displacement that controls the pulses of T_5.

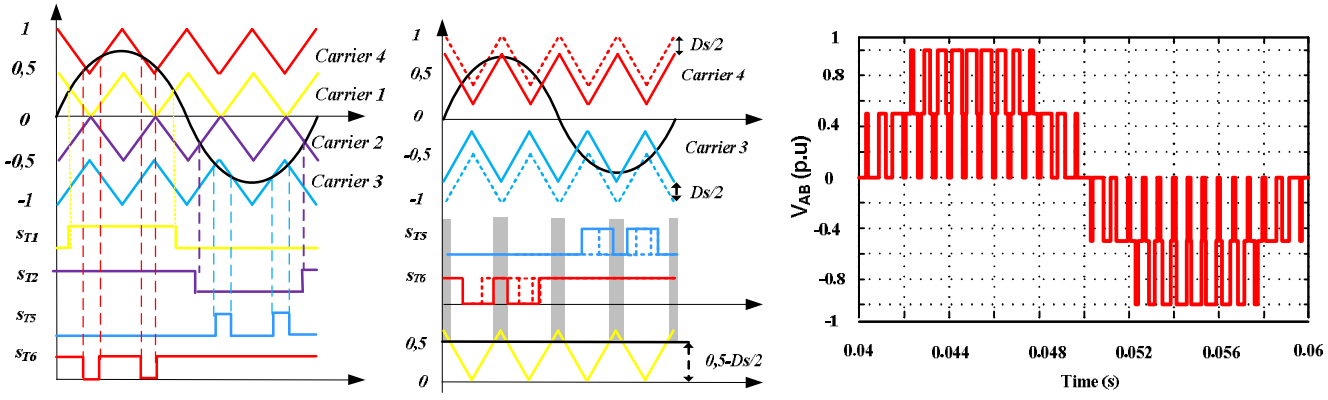
The resulting waveform of the output voltage before the output filter is shown schematically in Fig. 5 *c*.

B. Boost Regulation Capability

In the proposed modulation technique the desired boost is reached because the shoot-through states are distributed with a constant width during the whole output voltage period and the qZ stage is working at the maximum frequency.

Furthermore, by this technique we can use the ratio between the modulation index and the shoot-through duty cycle $M=1-D_S$ and the ratio between *B* and D_s (53) the RMS output voltage V_{OUT} can be estimated as

$$V_{OUT} = V_{IN} \cdot \frac{1-D_S}{\sqrt{2} \cdot (1-2 \cdot D_S)}. \quad (62)$$



(a) (b) (c)

Fig. 5. Sketch of the proposed modulation technique with uniformly distributed shoot-through states and constant width.